

Model Name: GA-P85-D3

1.1

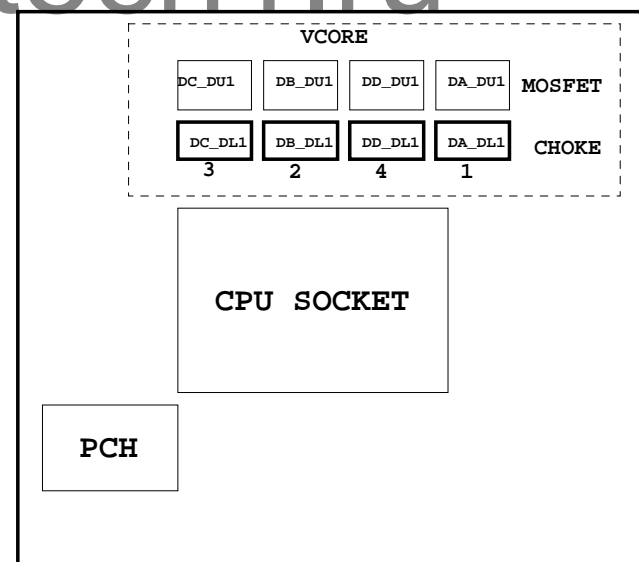
SHEET TITLE

01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	CPU_LGA1150-A
05	CPU_LGA1150-B
06	CPU_LGA1150-C
07	DDR III CHANNEL A
08	DDR III CHANNEL B
09	PCH_FDI,DMI,USB,PCIE
10	PCH_RGB,CLK BUFFER
11	PCH_HOST,SATA,PCI
12	PCH_GPIO,CTRL,AUDIO
13	PCH_PWR,GND
14	PCI EXPRESS*16 SLOT
15	PCIEX1*1 , PCIEX4 SLOT
16	ITE8892 PCI BRIDGE
17	PCI SLOT 1~4
18	I/O ITE8728
19	COM, -PROHOT, R_USB
20	Dual BIOS / LPT
21	ALC887 CODEC
22	REAR AUDIO JACK
23	VCORE_ ISL95820_1
24	VCORE_ ISL95820_2
25	DDR15V / M3 POWER
26	NCP3933 OVER VOLTAGE
27	DISCRETE POWER

SHEET TITLE

28	F_PANEL , F_USB2.0/3.0
29	ATX POWER, CLOCK GEN
30	HWM , KB/MS , FAN CTRL
31	Realtek 8111F-VL
32	HDMI
33	TABLE LIST
34	
35	
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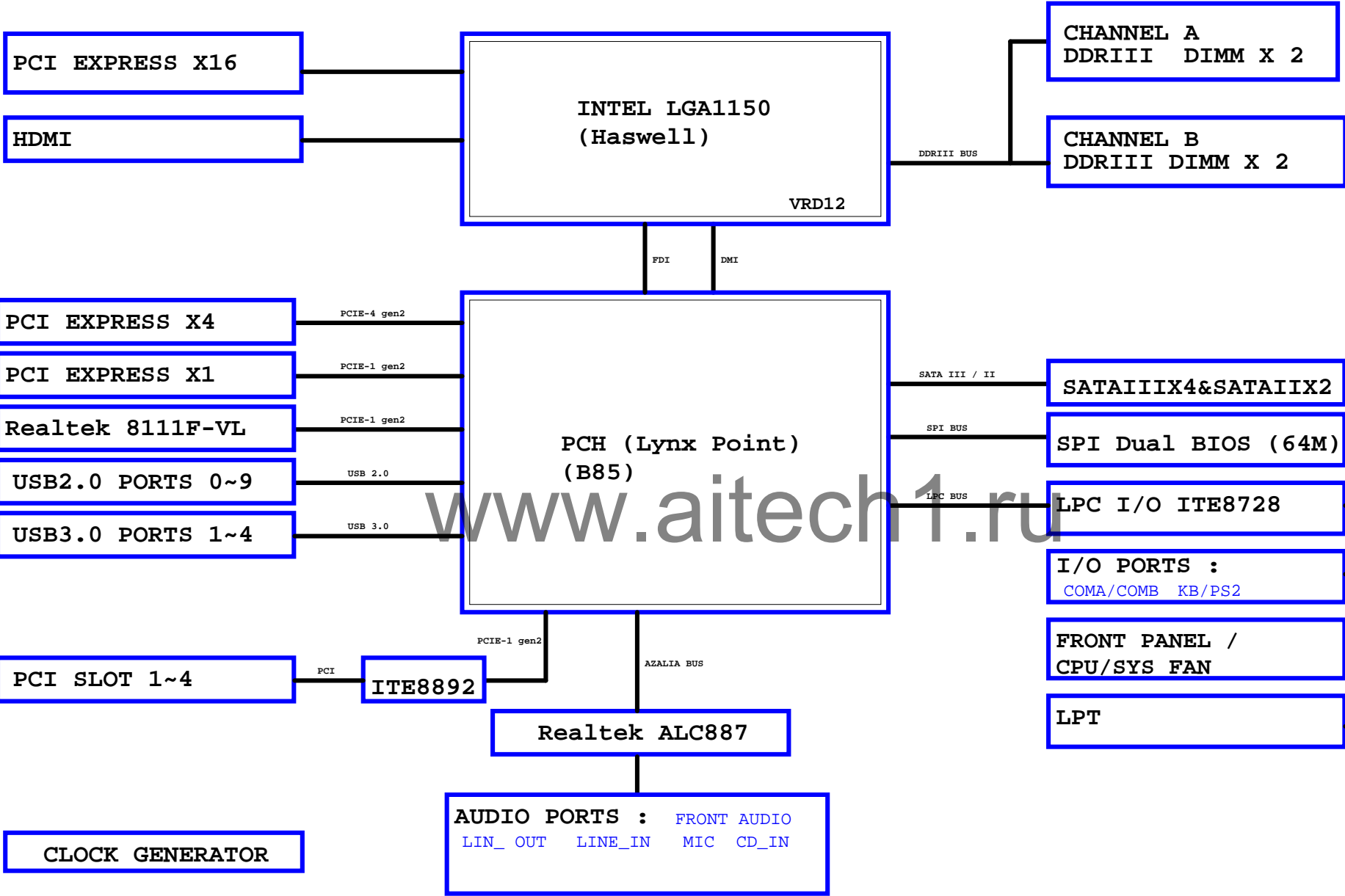
www.aitech1.ru



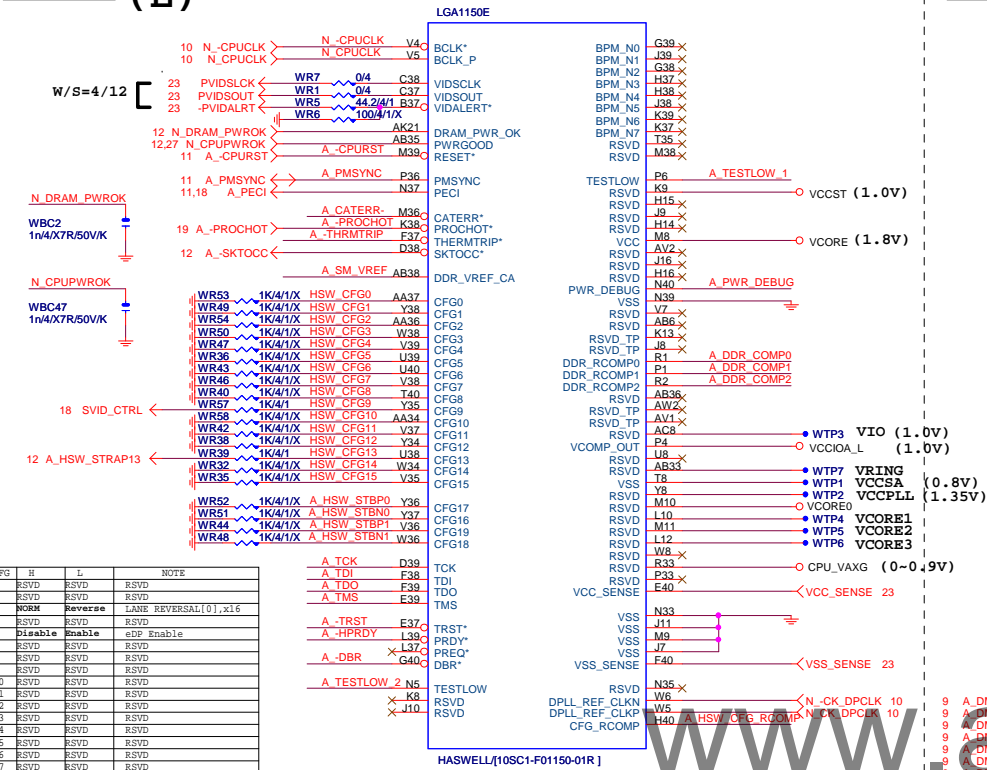
Component value change history

[illegible][illegible]

BLOCK DIAGRAM



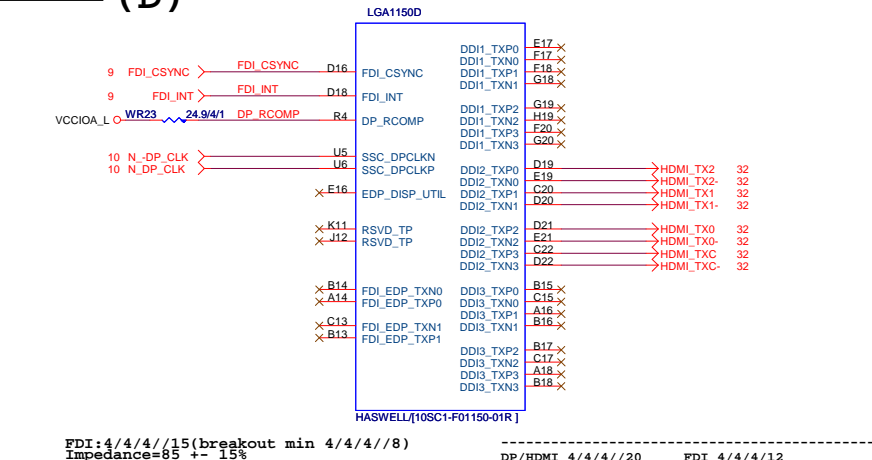
LGA1150 (E)



CFG6	CFG5	PCIE CONFIG
1	1	1x16 , Default
1	0	2x8
0	1	RSVD
0	0	X8, X4, X4

G 0-17 all internal PULL-UP

LGA1150 (D)



DP/HDMI 4/4/4//20 FDI 4/4/4/12

Impedance=85 +- 15%

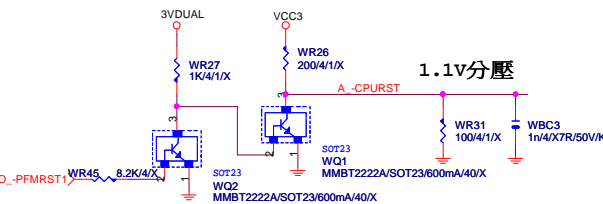
LGA1155 (C)



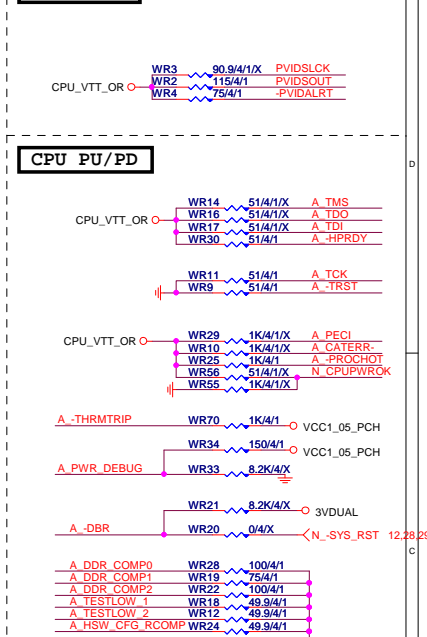
CPU PEG 5/5/5//20 Impedance=80 +- 15%

DMI 4/4/4//15 Impedance=85 +- 15%

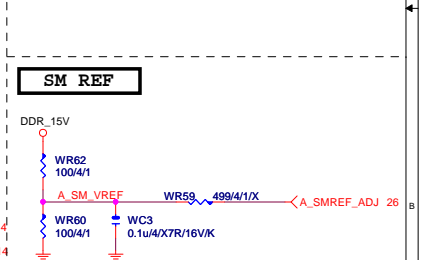
-CPURST

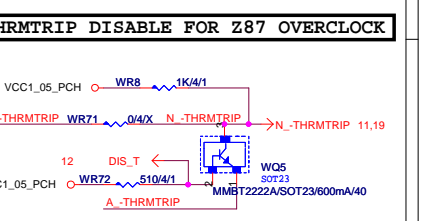


CPU SVID

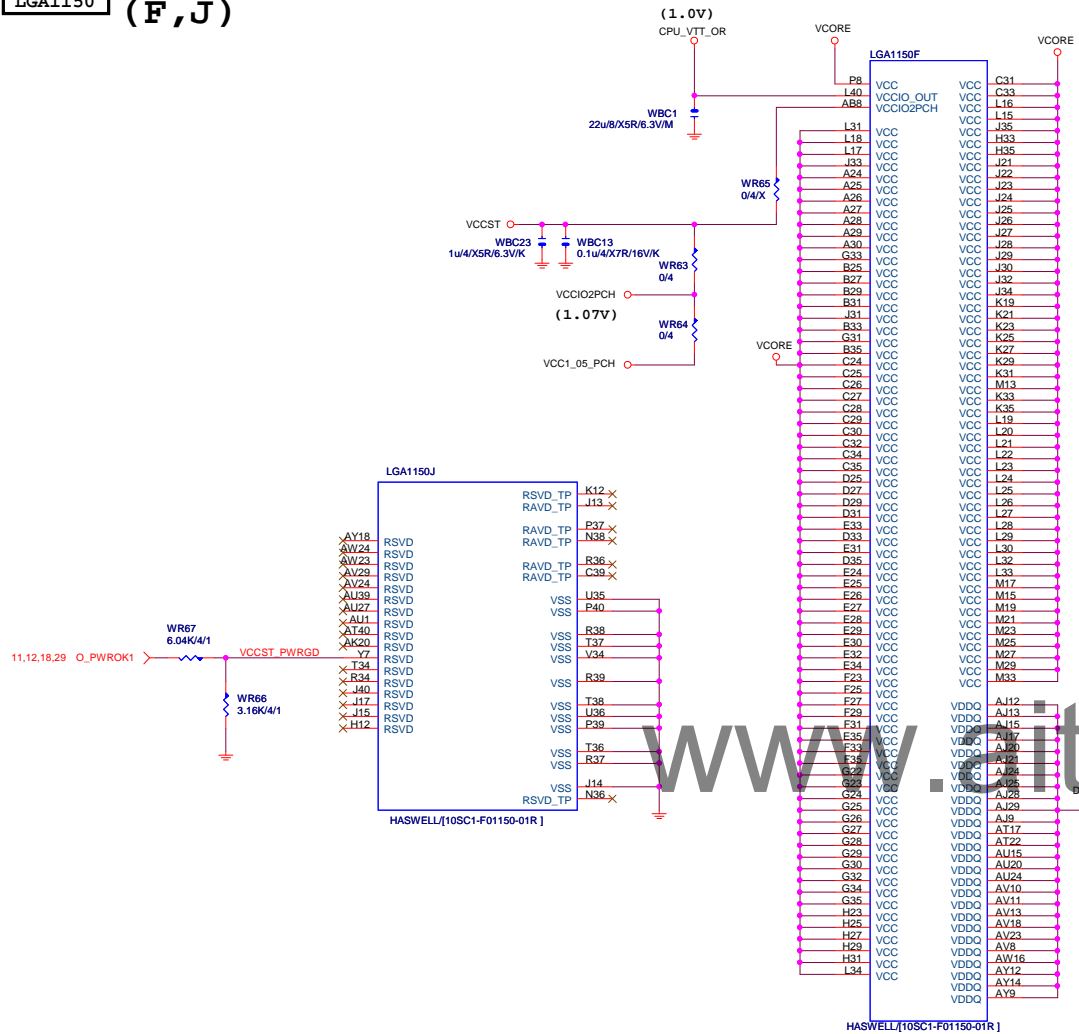


1





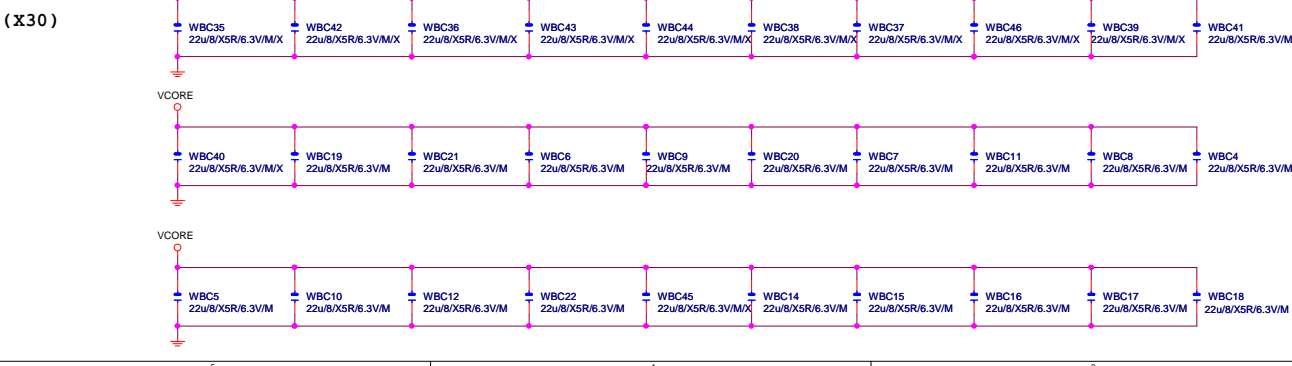
LGA1150 (F,J)



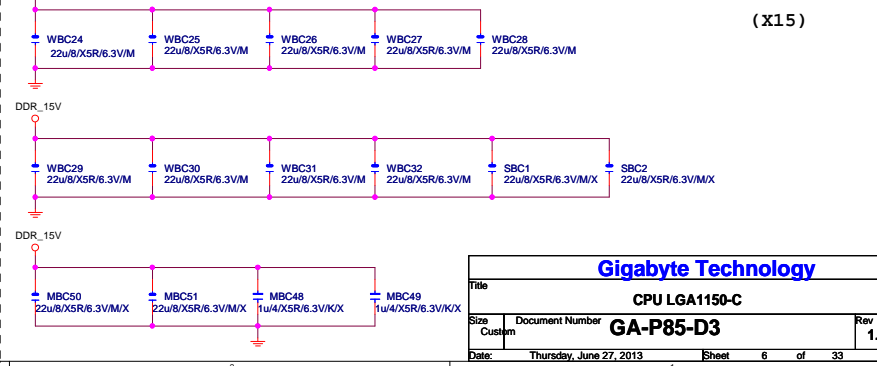
LGA1150 (G,H,I)

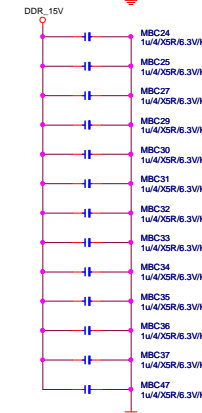
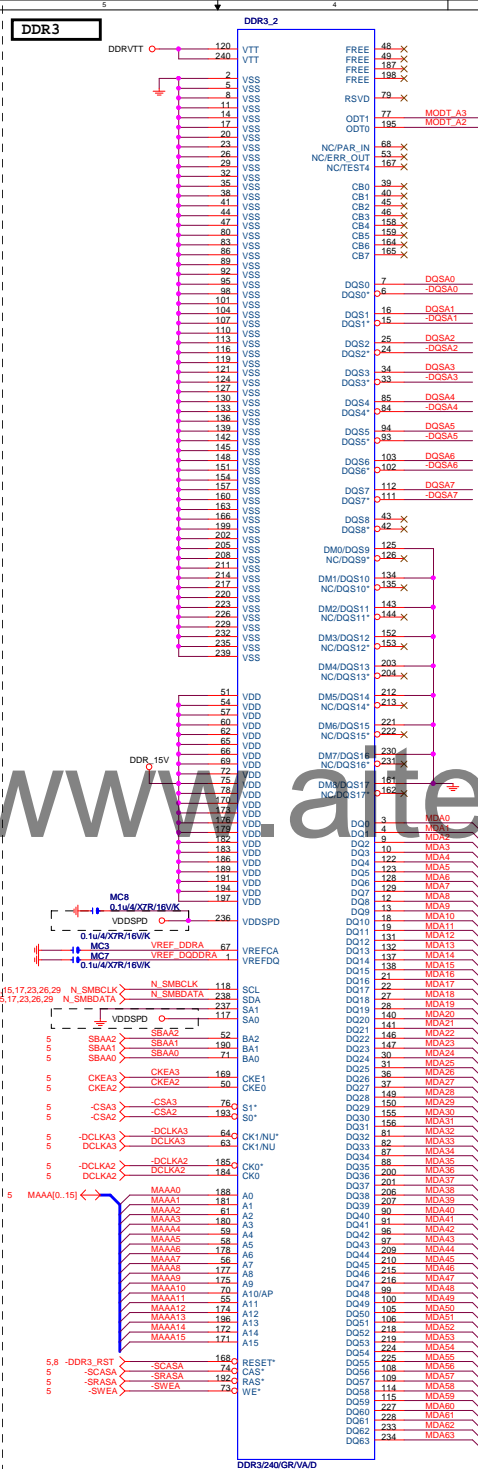


VCore CAP



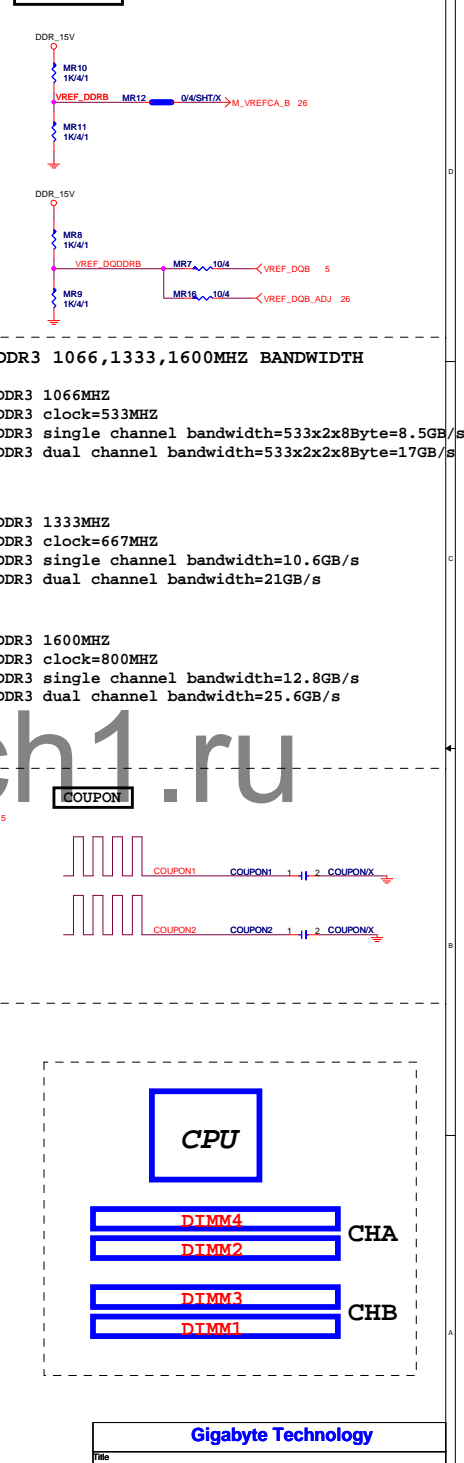
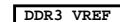
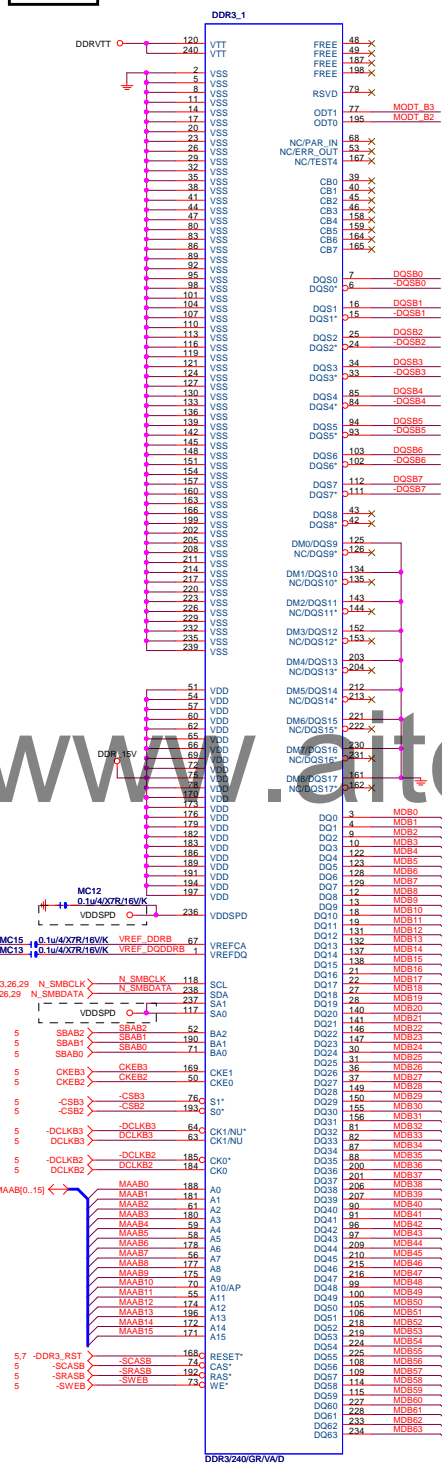
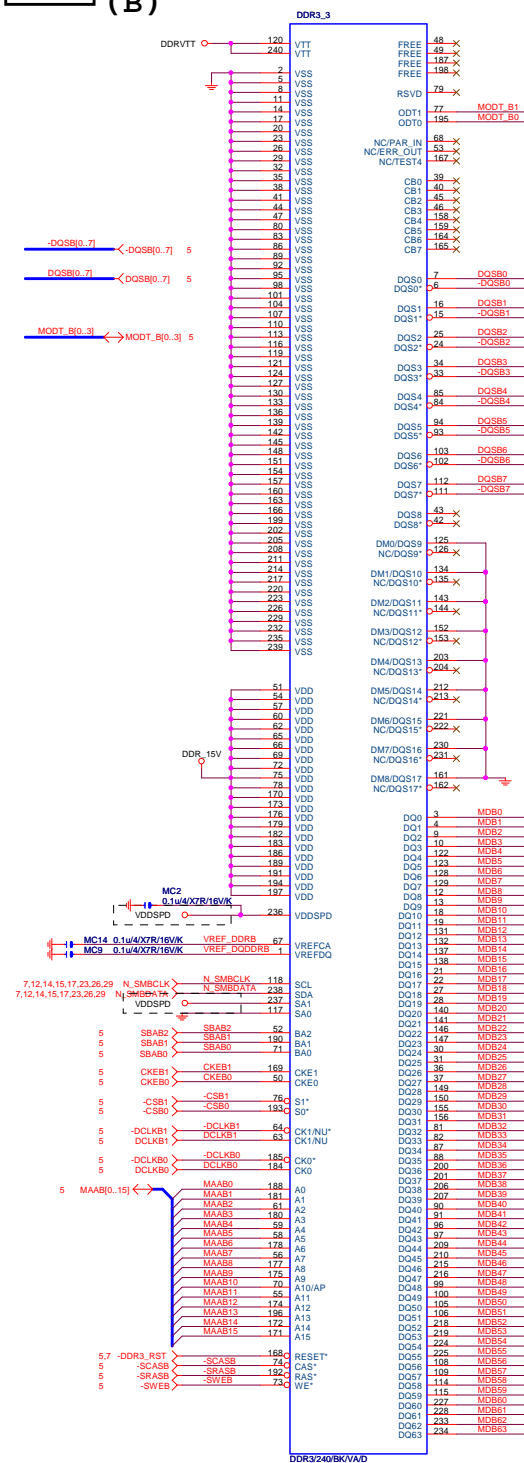
DDR CAP







(B)



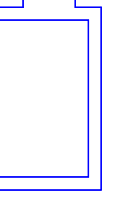
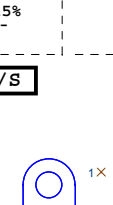
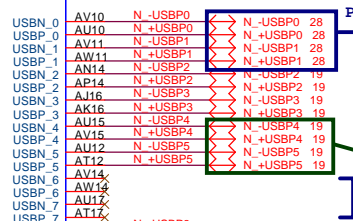
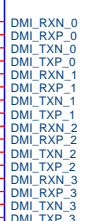
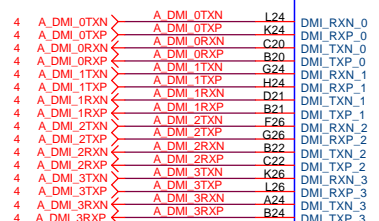
PCH

(B)

DMI:12/4/4/12(breakout min 8/4/4/4/8)
Impedance=85 +- 17.5%

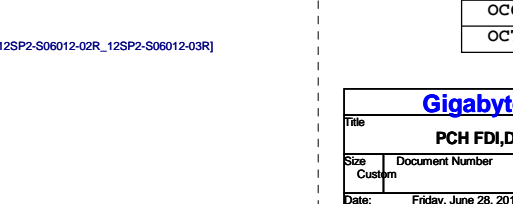
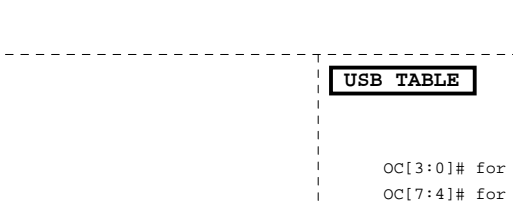
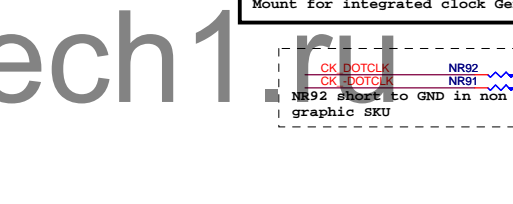
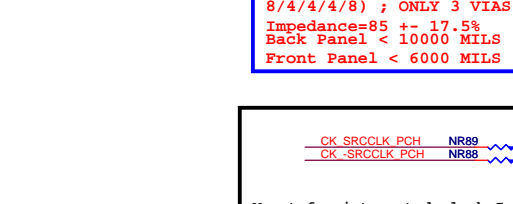
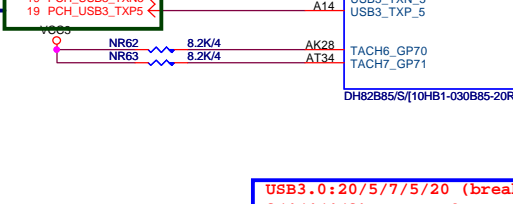
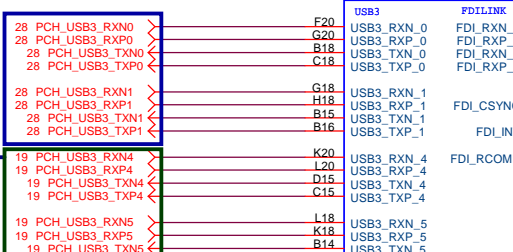
USB2.0 : 12/5/7/5/12 (breakout min 8/4/4/4/8)

Impedance=85 +- 15%

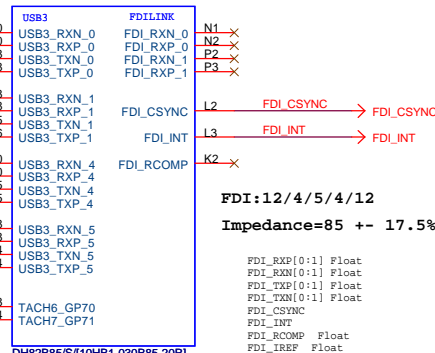


PCH

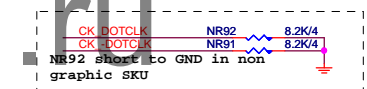
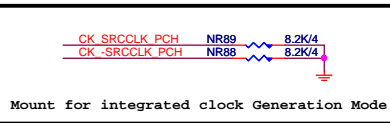
(F)



PCHF

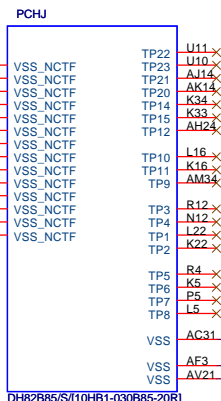


USB3.0:20/5/7/5/20 (breakout min 8/4/4/4/8) ; ONLY 3 VIAS
Impedance=85 +- 17.5%
Back Panel < 10000 MILS
Front Panel < 6000 MILS



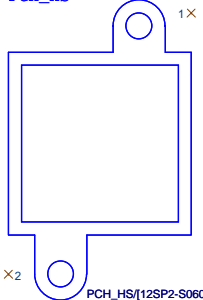
PCH

(J)



PCH H/S

PCH_HS



USB TABLE

OC[3:0]# for Device 29 (ports 0-7)
OC[7:4]# for Device 26 (ports 8-13)

USB OC# Configure	
OC0#	USB0,1
OC1#	USB2,3
OC2#	USB4,5
OC3#	USB6,7
OC4#	USB8,9
OC5#	USB10,11
OC6#	USB12,13
OC7#	Not Use

Gigabyte Technology

Gigabyte Technology			
Title			
PCH FDI,DMI,USB ,PCIE			
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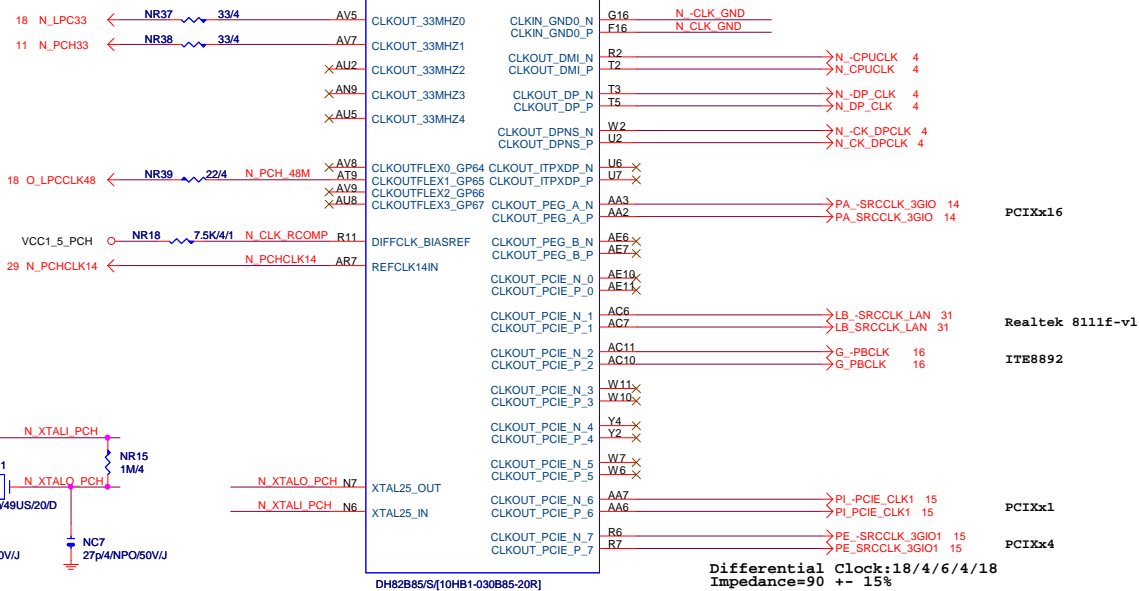
CLOSE SLOPE PCH<0.75";4/10;+-1000;GND

DDBP_HPD VGA_HS SYNC AH3 ✕
DDPC_HPD VGA_VS SYNC AH2 ✕
DDBP_HPD AC2
VGA_RED AC3
DDBP_AUXN VGA_GREEN
DDPC_AUXP VGA_BLUE
DDBP_AUXP AG4
DDPC_AUXP AE2 N DDCDATA DDC DIFF 4/5;+-1000
DDBP_AUXP VGA_IRTN
VGA_DDC_DATA AL3 N DDCLK
VGA_DDC_CLK AL2 N DDCLK
DAC_IREF AF5 N VGA RESET NR34 04SHIT/MK IREF 4/12;<500MILS;GND
DDBP_CTRLCLK AN3 N DDPC CTRLCLK 32
DDPC_CTRLDATA AM2 N DDPC CTRLDATA 32
DDBP_CTRLDATA AM1 ✕
DDBP_CTRLCLK AJ5 ✕
DDBP_CTRLCLK AN4 ✕
DDBP_CTRLDATA AN2 ✕

DH82B85/[10HB1-030B85-20R]

VGA_DISABLE
R,G,B NC OR GND
IRTN / IREF GND
VGA_HS SYNC, VGA_VS SYNC, DDC_CLK,
DDC_DATA NC
POWER VCCADAC(AF2),
VCCADACBG(AE1) GND

Flex1,2,3,4 :
14/24/33/48MHZ

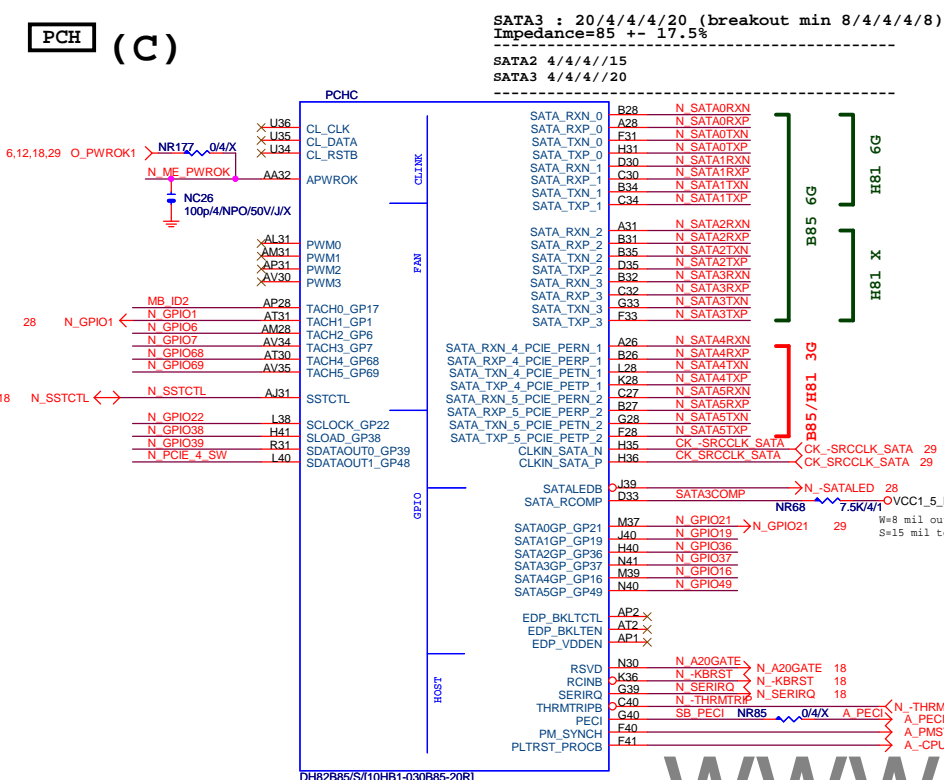


Mount for integrated clock Generation Mode

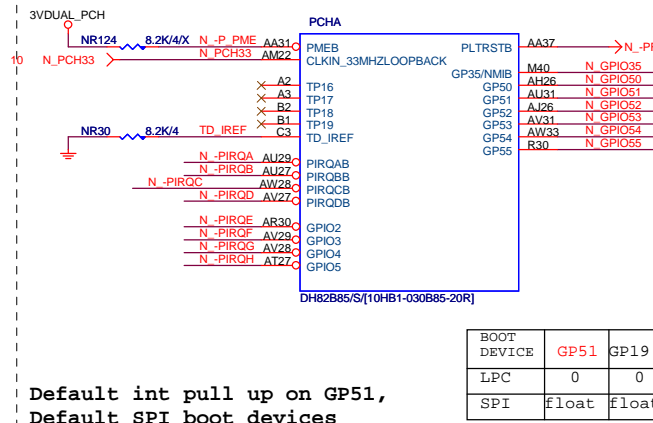
VGA DDC

Gigabyte Technology				
Title				
PCH DISPLAY ,CLK BUFFER				
Size	Document Number			Rev
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PCH (C)



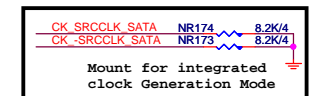
PCH (A)



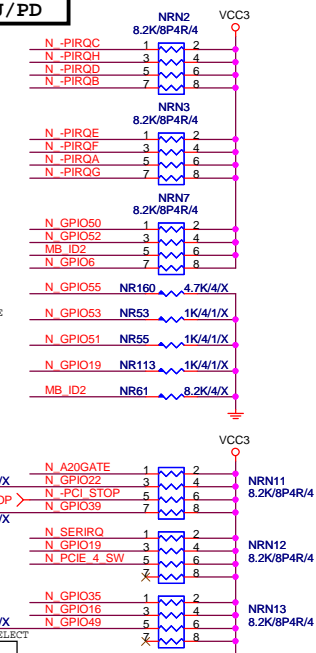
```
Default int pull up on GP51,
Default SPI boot devices
```

BOOT DEVICE	GP51	GP19
LPC	0	0
SPI	float	float

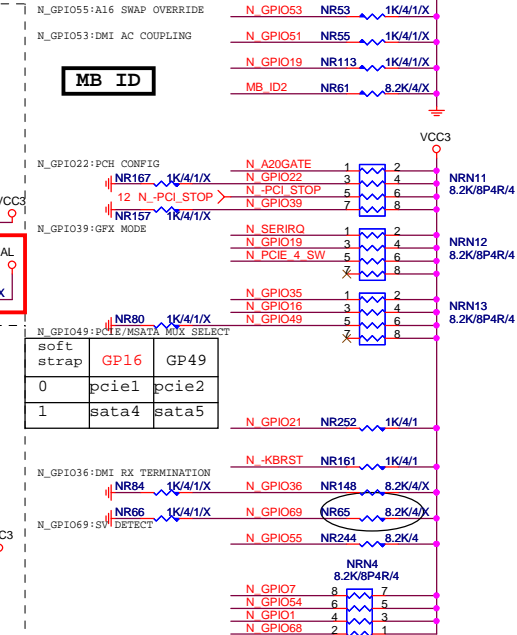
PCH CLK PD



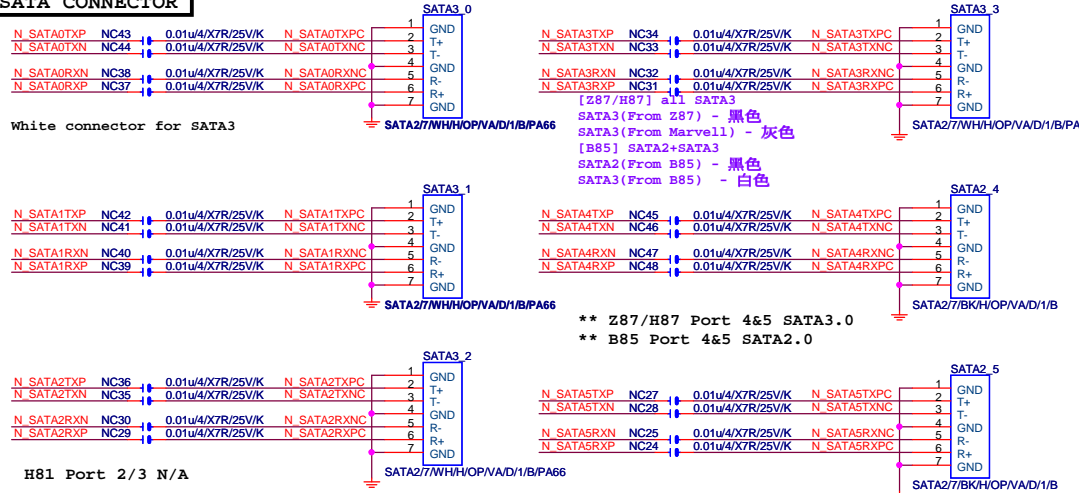
PCH PU/PD



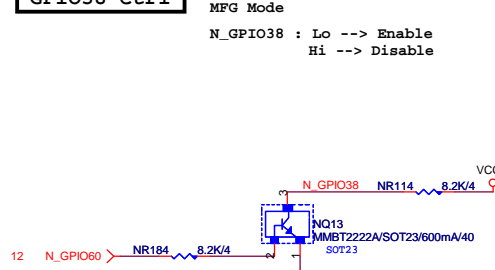
MB ID



SATA CONNECTOR



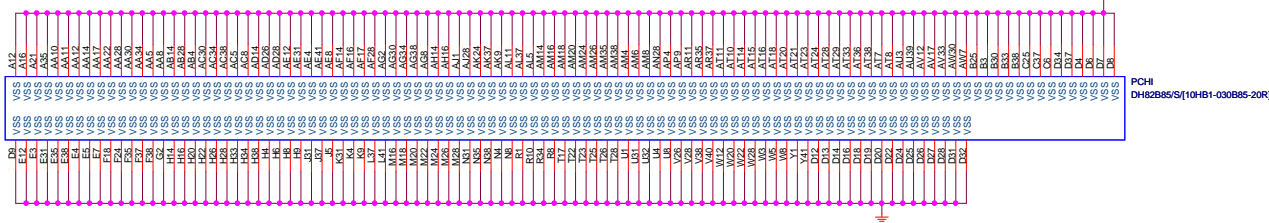
GPIO38 Ctrl



```
MFG Mode

N_GPIO38 : Lo --> Enable
           Hi --> Disable
```

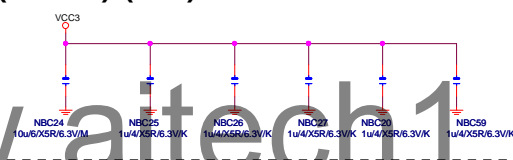

PCH (I)



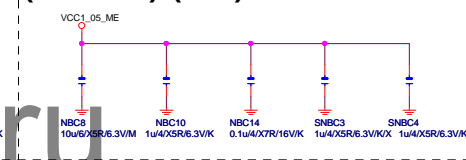
SHT PWR

The figure shows two circuit diagrams for NR pin connections. The top diagram shows NR5 connected to VCC3_ME and NR6 connected to VCC3, with a 0/8P4R/4/X component in between. The bottom diagram shows NR1 connected to VCC1_05_ME and NR2 connected to VCC1_05_PCH, also with a 0/8P4R/4/X component in between.

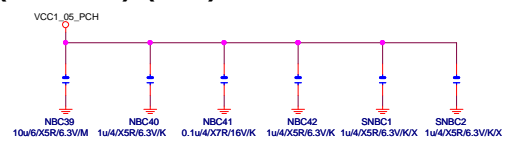
(3.3V) (X6)



(1.05V) (x5)



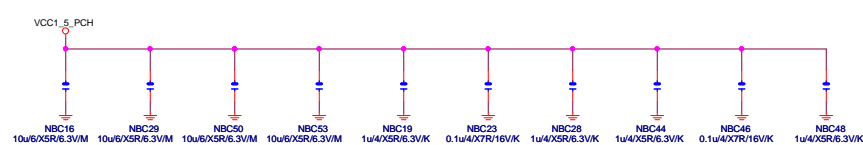
(1.05V) (x6)



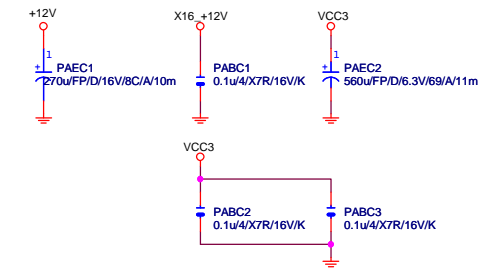
(1.05V)(X2) (3.3V) (X2)



(1.5V) (x10)

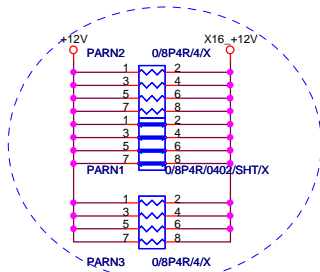


PCIEX16 CAP



PCIEX16 PROTECT SHT

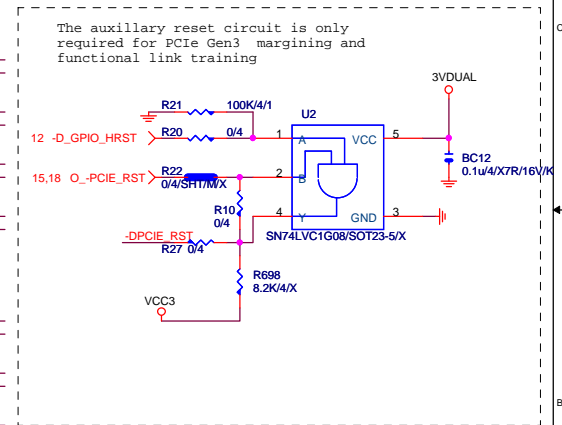
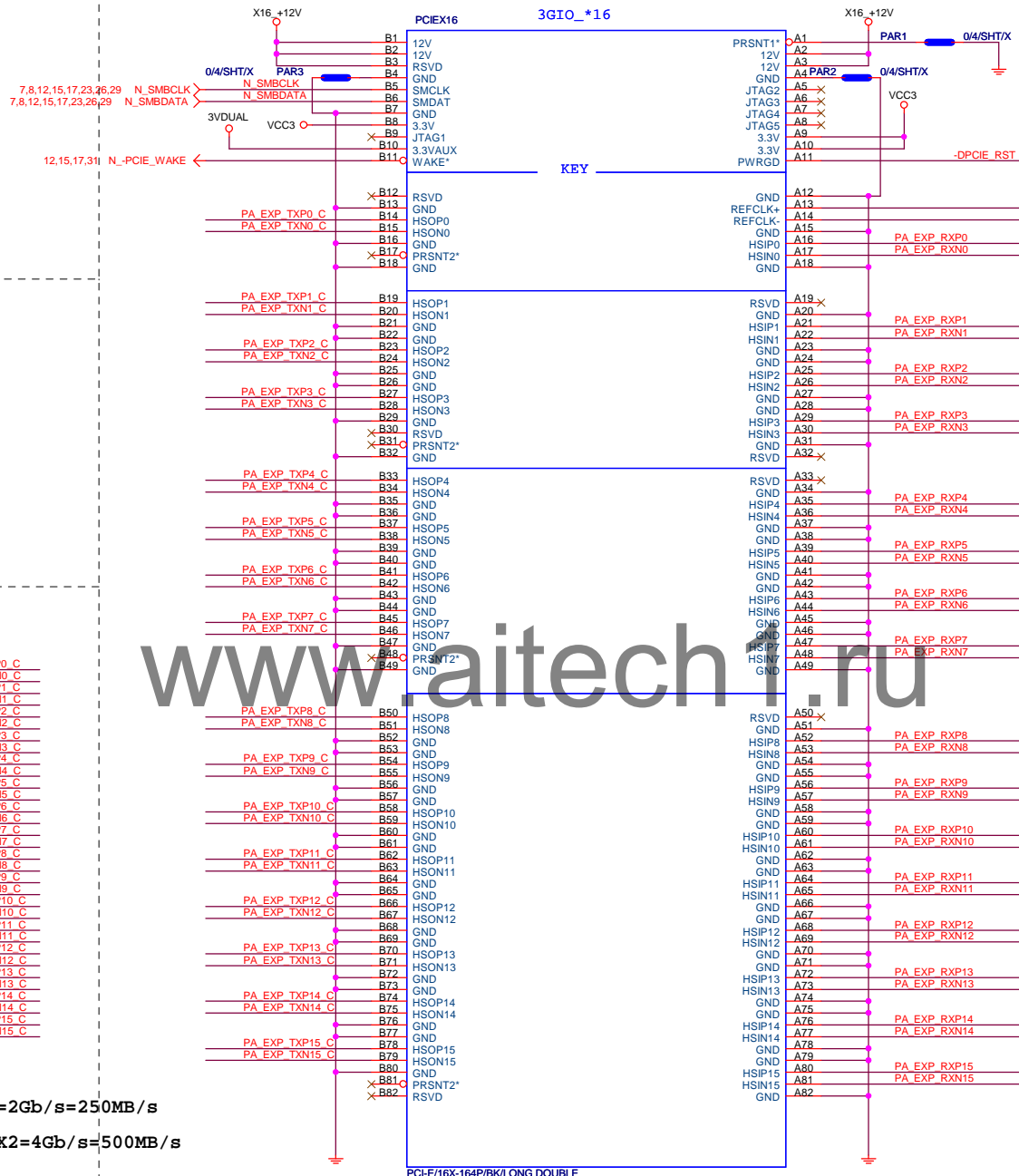
+12 protect short-wire test



PCIEX16 AC CAP

PA EXP TXP0	PAC5	0.22u4/X5R/6.3V/K	PA EXP TXP0 C
PA EXP TXN0	PAC4	0.22u4/X5R/6.3V/K	PA EXP TXN0 C
PA EXP TXP1	PAC6	0.22u4/X5R/6.3V/K	PA EXP TXP1 C
PA EXP TXN1	PAC7	0.22u4/X5R/6.3V/K	PA EXP TXN1 C
PA EXP TXP2	PAC8	0.22u4/X5R/6.3V/K	PA EXP TXP2 C
PA EXP TXN2	PAC9	0.22u4/X5R/6.3V/K	PA EXP TXN2 C
PA EXP TXP3	PAC10	0.22u4/X5R/6.3V/K	PA EXP TXP3 C
PA EXP TXN3	PAC11	0.22u4/X5R/6.3V/K	PA EXP TXN3 C
PA EXP TXP4	PAC12	0.22u4/X5R/6.3V/K	PA EXP TXP4 C
PA EXP TXN4	PAC13	0.22u4/X5R/6.3V/K	PA EXP TXN4 C
PA EXP TXP5	PAC14	0.22u4/X5R/6.3V/K	PA EXP TXP5 C
PA EXP TXN5	PAC15	0.22u4/X5R/6.3V/K	PA EXP TXN5 C
PA EXP TXP6	PAC16	0.22u4/X5R/6.3V/K	PA EXP TXP6 C
PA EXP TXN6	PAC17	0.22u4/X5R/6.3V/K	PA EXP TXN6 C
PA EXP TXP7	PAC19	0.22u4/X5R/6.3V/K	PA EXP TXP7 C
PA EXP TXN7	PAC18	0.22u4/X5R/6.3V/K	PA EXP TXN7 C
PA EXP TXP8	PAC20	0.22u4/X5R/6.3V/K	PA EXP TXP8 C
PA EXP TXN8	PAC21	0.22u4/X5R/6.3V/K	PA EXP TXN8 C
PA EXP TXP9	PAC22	0.22u4/X5R/6.3V/K	PA EXP TXP9 C
PA EXP TXN9	PAC23	0.22u4/X5R/6.3V/K	PA EXP TXN9 C
PA EXP TXP10	PAC24	0.22u4/X5R/6.3V/K	PA EXP TXP10 C
PA EXP TXN10	PAC25	0.22u4/X5R/6.3V/K	PA EXP TXN10 C
PA EXP TXP11	PAC26	0.22u4/X5R/6.3V/K	PA EXP TXP11 C
PA EXP TXN11	PAC27	0.22u4/X5R/6.3V/K	PA EXP TXN11 C
PA EXP TXP12	PAC28	0.22u4/X5R/6.3V/K	PA EXP TXP12 C
PA EXP TXN12	PAC29	0.22u4/X5R/6.3V/K	PA EXP TXN12 C
PA EXP TXP13	PAC30	0.22u4/X5R/6.3V/K	PA EXP TXP13 C
PA EXP TXN13	PAC31	0.22u4/X5R/6.3V/K	PA EXP TXN13 C
PA EXP TXP14	PAC32	0.22u4/X5R/6.3V/K	PA EXP TXP14 C
PA EXP TXN14	PAC33	0.22u4/X5R/6.3V/K	PA EXP TXN14 C
PA EXP TXP15	PAC34	0.22u4/X5R/6.3V/K	PA EXP TXP15 C
PA EXP TXN15	PAC35	0.22u4/X5R/6.3V/K	PA EXP TXN15 C

PCIEX16 SLOT



PCIEX16:16/5/5/5/16

PA EXP RXP0[0..15]	>>>PA_EXP_RXP[0..15]	4
PA EXP RXN0[0..15]	>>>PA_EXP_RXN[0..15]	4
PA EXP TXP0[0..15]	>>>PA_EXP_TXP[0..15]	4
PA EXP TXN0[0..15]	>>>PA_EXP_TXN[0..15]	4

PCI-E REV:1.1--> 2.5GHZ

PCE-E X1(單向) BANDWITH=2.5GHz*(8b/10b)=2Gb/s=250MB/s

PCE-E X1(雙向) BANDWITH=2.5GHz*(8b/10b)X2=4Gb/s=500MB/s

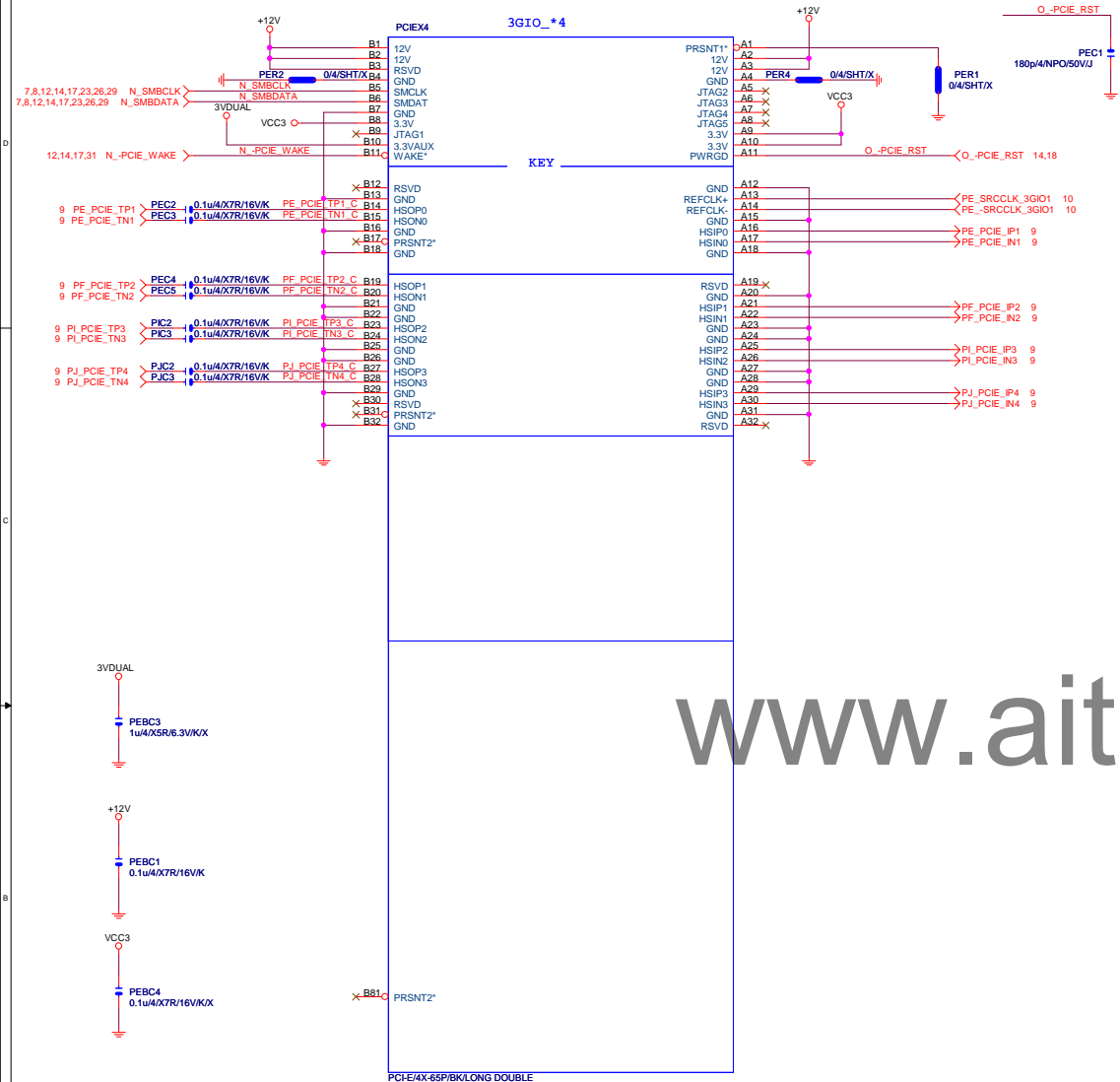
PCE-E X16(單向) BANDWITH=2.5GHz*(8b/10b)X16=32Gb/s=4GB/s

PCE-E X16(雙向) BANDWITH=2.5GHz*(8b/10b)X16X2=64Gb/s=8GB/s

PCI-E REV:2.0--> 5GHZ

Gigabyte Technology		
PCI EXPRESS * 16		
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PCIEX4 SLOT

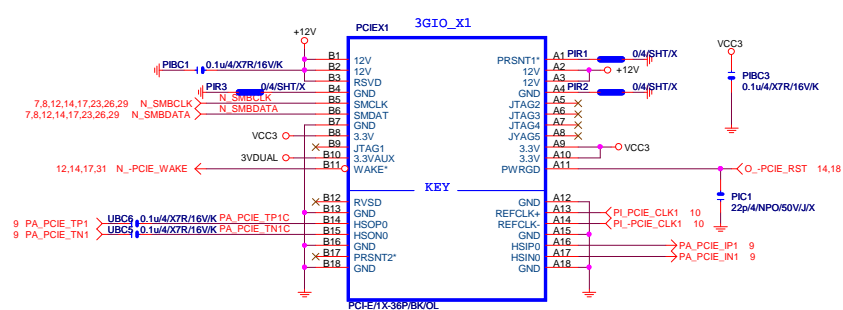


PCI-E/AX-65P/BK/LONG DOUBLE

	N_PCIE_4_SW (PCH_GPIO48)	PCIEX4_X1 (SIO_GPIO26)
P	H	H
C	H	H
PCIEX4 No devices	H	H
PCIEX4 -> X1	H	H
PCIEX4 Have devices	L	L
PCIEX4 -> X4	L	L
PCIEX1_1/2 --> N/A		

PCIEX1 SLOT

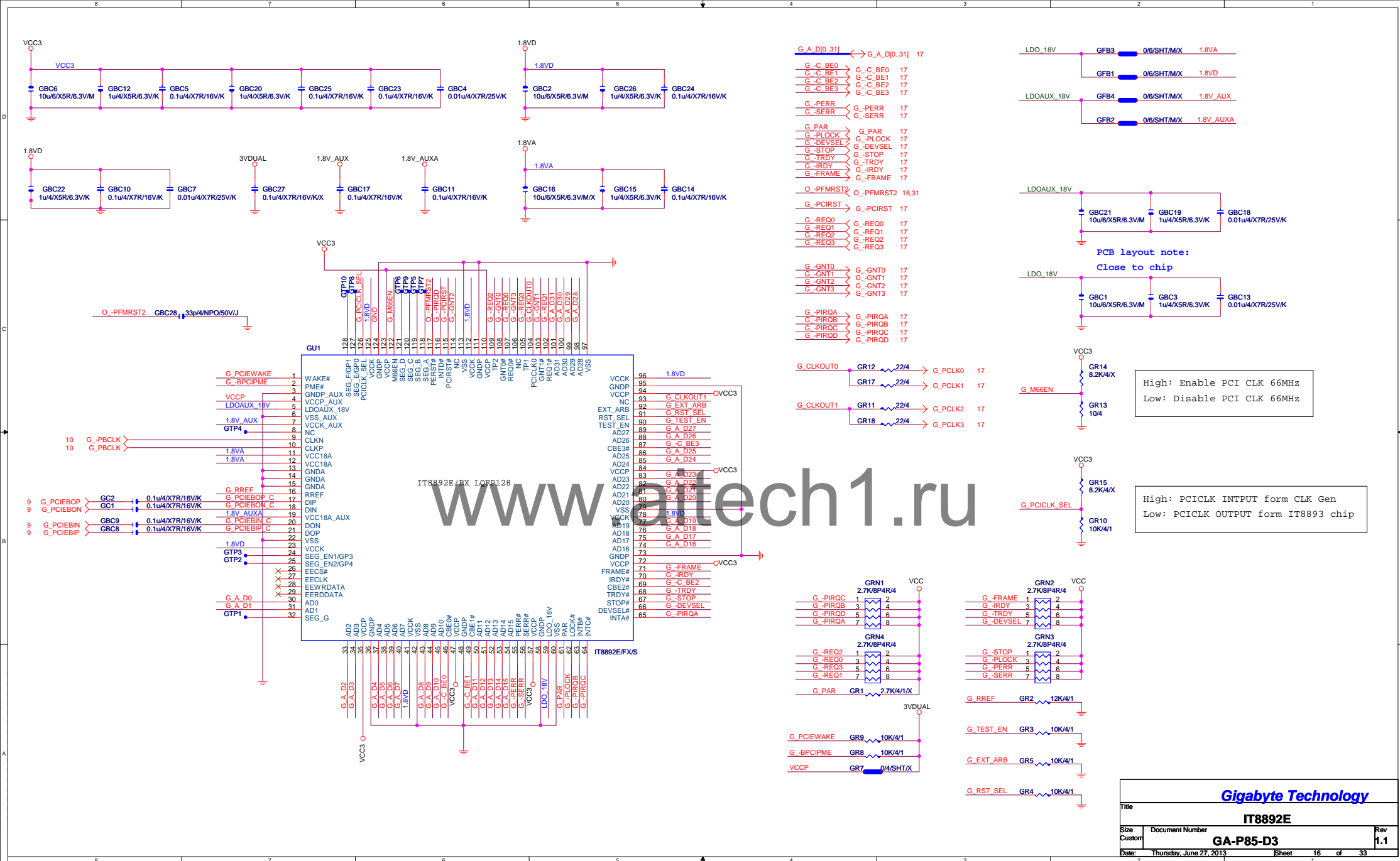
PCIEX1_1



PCIEX4/X1 SWITCH

Function	SEL
x1--> x0a	L;PCIEX4 SLOT-->X1
x1--> x0b	H;PCIEX4 SLOT-->X4

Gigabyte Technology			
Title	PCI X1 1,2		
Size	Document Number	Rev	
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SIO IT8728F

SYS_FAN3

DS_ME
IO_GP22
MPD+

CPU_OPT

CPU_FAN

SYS_FAN1

SYS_FAN2

IT8728F (GB)

【技術通報R&D技術通報151】
有使用PRINT PORT的 MODEL
需使用新料號:10HP2-118728-72R

PWR SHT

For 8728_EUP function
3VDUAL_PCH OR25 0/6SHT/X IT_VCCH
VCC3 OR49 0/6SHT/X IT_AVCC

SIO PU

SVID_CTRL OR84 8.2K/4 3VDUAL_PCH
-5VSB_CTRL OR6 8.2K/4 3VDUAL_PCH
-THERM OR28 8.2K/4 VCC3
N_LDRQ0 OR27 1K/4/1 VCC3
ITE_PWROK2 OR16 1K/4/1 VCC3
ITE_PWROK OR10 1K/4/1 VCC3
O_-PCIE_RST OR71 1K/4/1 VCC3
O_-PFMRST1 OR19 1K/4/1 VCC3
O_-PFMRST2 OR2 1K/4/1 VCC3
N_A20GATE OR31 680/4/1 X
Hi :Disable WDT
Lo :Enable WDT to rest PWROK

SIO STRAP

JP3--- High SPI-Flash Disable
Low SPI-Flash Enable
OR33 1K/4/1 X JP2 OR36 8.2K/4 VCC3
OR80 8.2K/4/1 X JP3 OR35 8.2K/4 VCC3
JP4 OR32 8.2K/4 VCC3
JP5 N/A FOR 8728 DX
JP5:PULL DOWN FOR 8728 EX
anti-surge enable
EUP control detect
3VDUAL_PCH OR47 100/4/1 28.3VSB

JP4	1	k8 power sequency function is Disable
	0	k8 power sequency function is Enable
JP3	1 1	The default value of EC Index 63h/6Bh/73h is 80h.
	0 1	The default value of EC Index 63h/6Bh/73h is FFh
JP5	0 1	The default value of EC Index 63h/6Bh/73h is 00h.
	0 0	The default value of EC Index 63h/6Bh/73h is 40h.

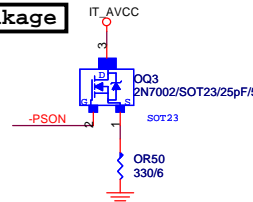
IT8728F NOTE

	IT8728
PIN121	VCORE_EN/PCH_C0
PIN120	VLDT_EN/PCH_D0
PIN19	ATXPG
PIN31	PCH_C1
PIN53	SST/AMDTST_D/MTRB#/PCH_D1
PIN55	PECI/AMDTST_C/DRV#
PIN66	SYS_3VSB
PIN70	GP47
PIN95	VIN2(VCC5)
PIN96	VIN1(VCC12)
PIN97	VIN1/VDIMM_STR(1.5V)
PIN98	VIN0/VCORE(1.1V)/NC

DUAL BIOS OPT STRAP

CEB_N OR58 680/4/1 X
OR56 1K/4/1 VCC3

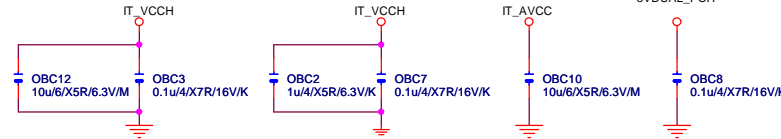
Power leakage



SIO_18V

internal power pin, max 22nF cap
SIO 18V
OBC4 0.1u4/X7R/16V/K X
OBC5 0.1u4/X7R/16V/K

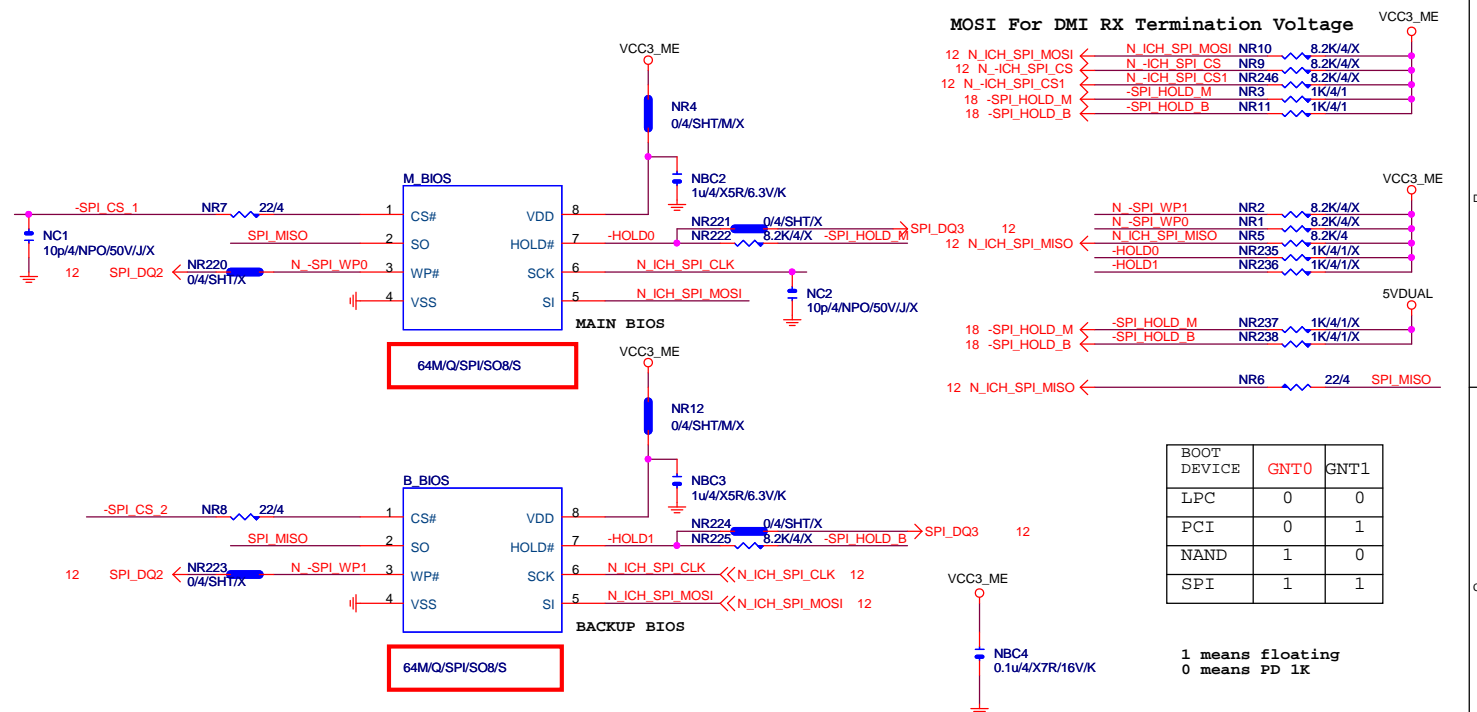
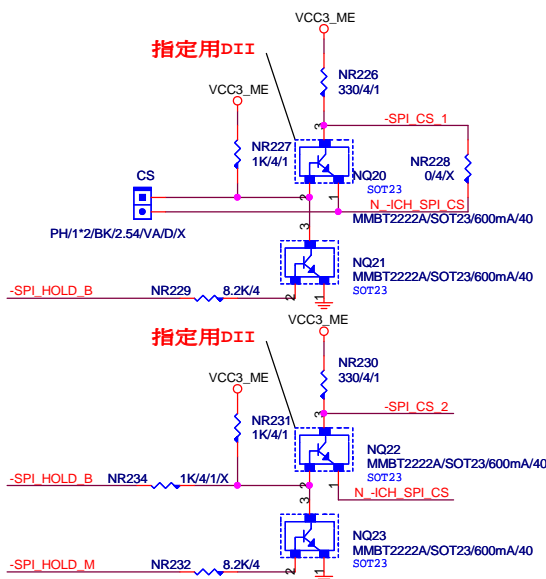
SIO CAP



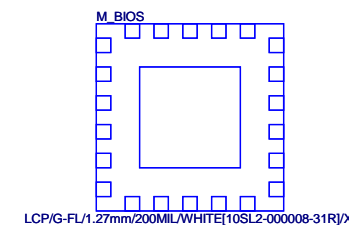
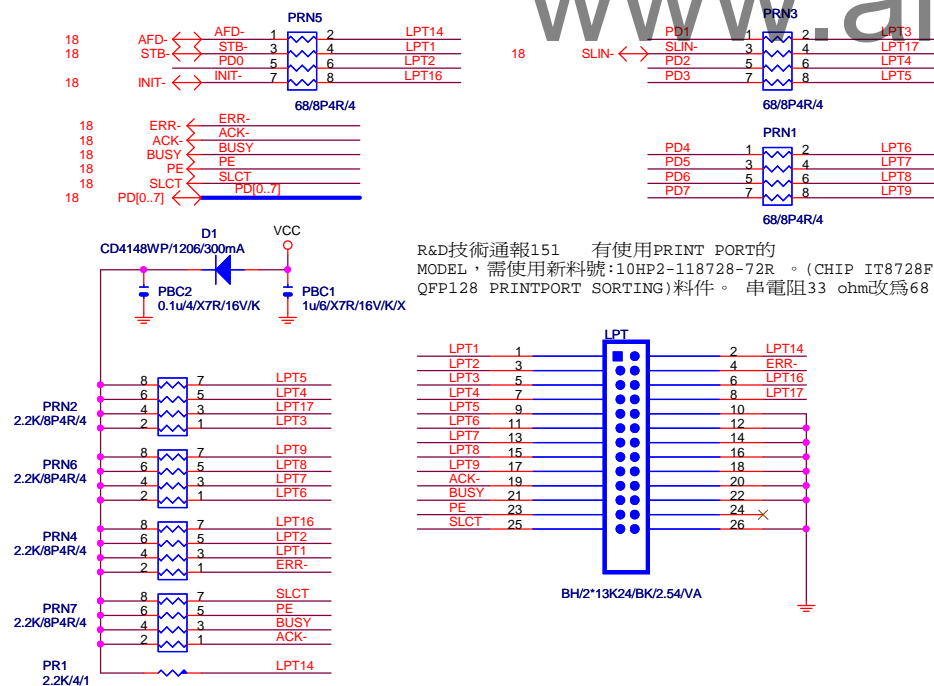
Gigabyte Technology

Title			ITE 8728 LPC IO
Size B	Document Number	GA-P85-D3	
Date:	Monday, July 01, 2013	Sheet	18 of 33
			Rev 1.1

DUAL BIOS



LPT PORT



R&D技術通報151 有使用PRINT PORT的
MODEL, 需使用新料號: 10HP2-118728-72R。(CHIP IT8728F/EX (GB) ITE/SMD
QFP128 PRINTPORT SORTING)料件。串電阻33 ohm改為68 ohm。

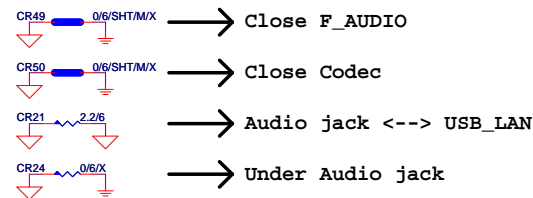
Gigabyte Technology

Title		BIOS	
Size Custom	Document Number	GA-P85-D3	Rev 1.1
Date:	Thursday, June 27, 2013	Sheet	20 of 33

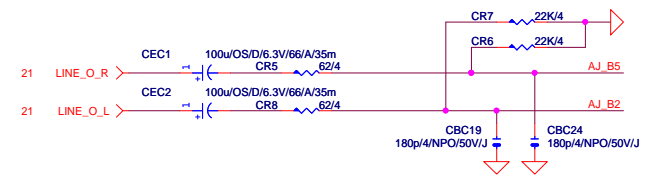
FOR ON/OFF PLAY



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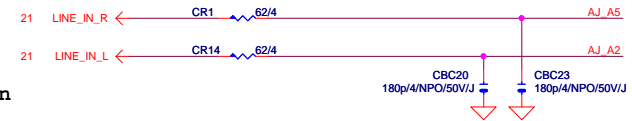
LINE-OUT



LINE-IN

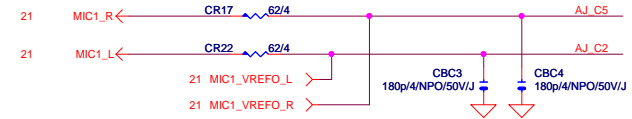
Verify MIC function
 in LINE-in

Only reserved for ALC888



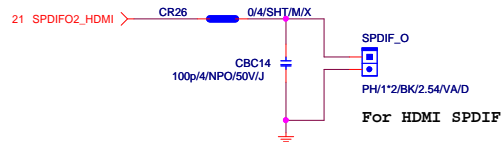
For 889A/888

MIC-IN

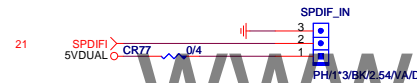


SURROUND

SPDIF_OUT



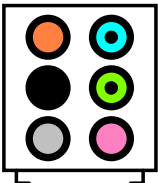
SPDIF_IN



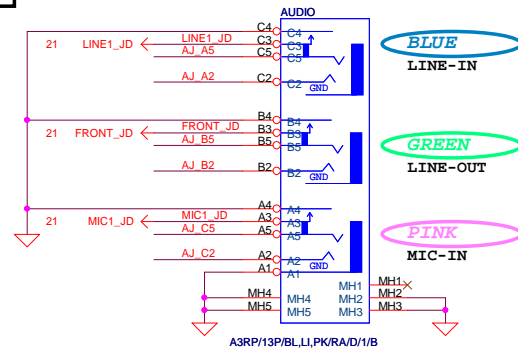
CEN/LFE

SURR BACK

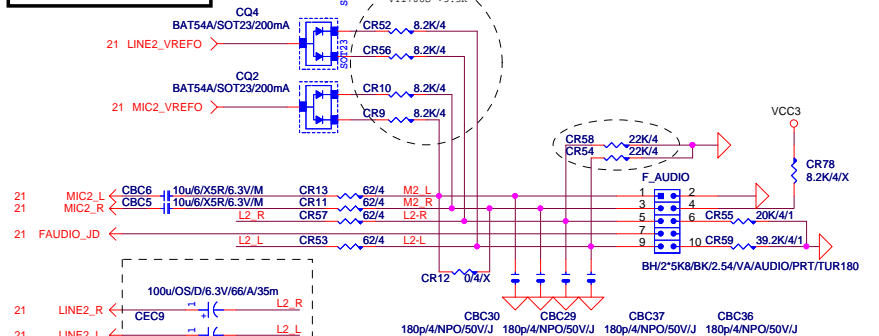
AZALIA JACK



AZALIA JACK



AZALIA FRONT PANEL



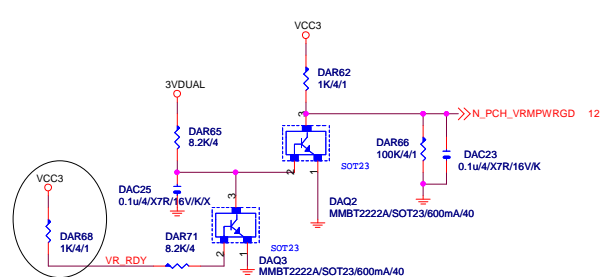
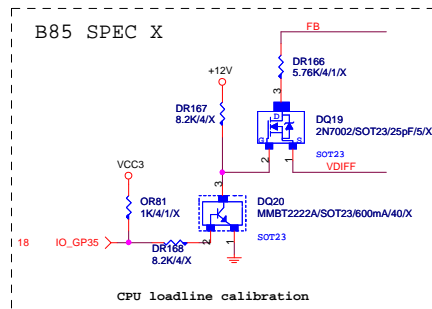
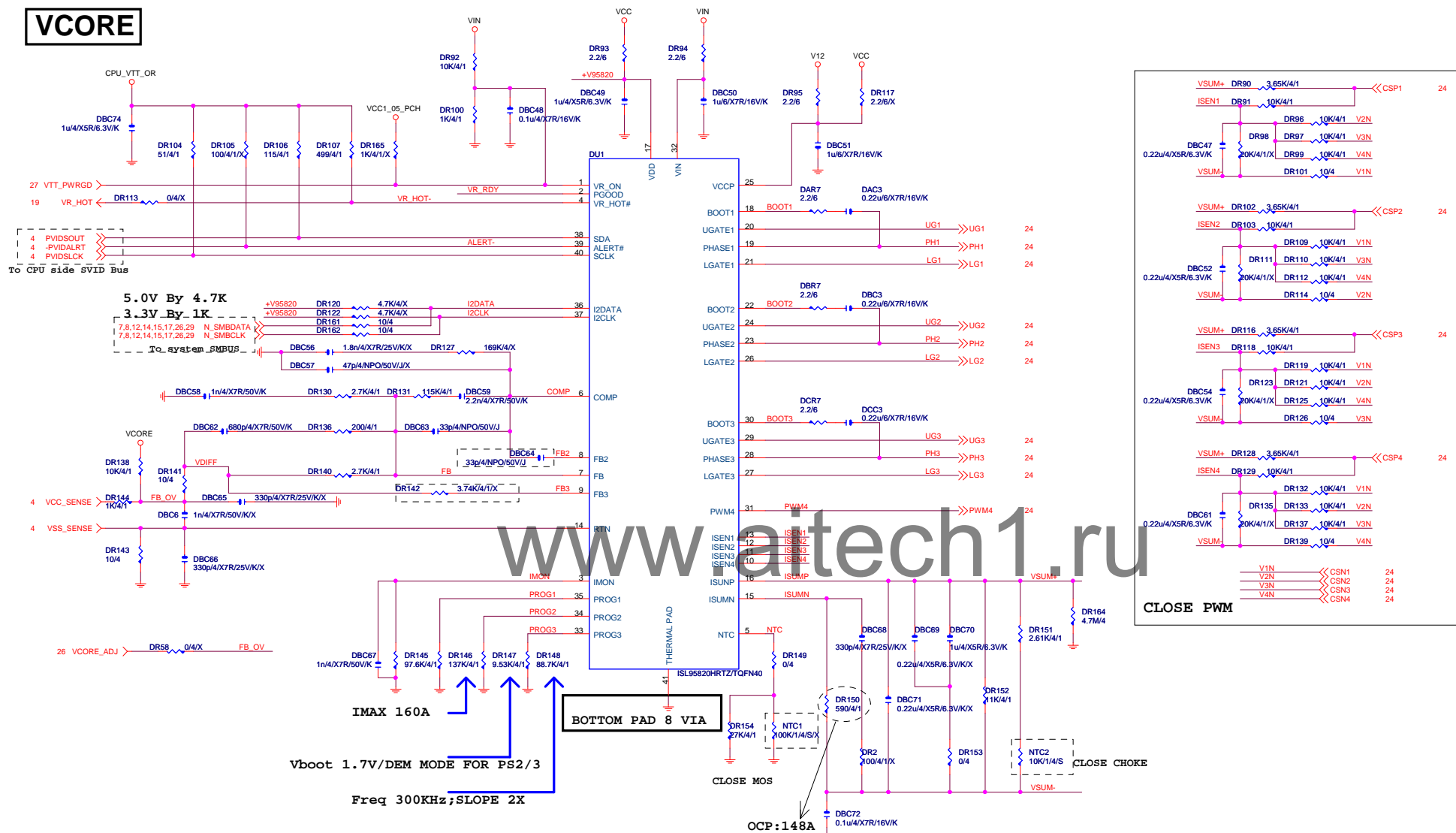
Gigabyte Technology

AUDIO JACK

GA-P85-D3

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Size Custom	GA-P85-D3	1.1
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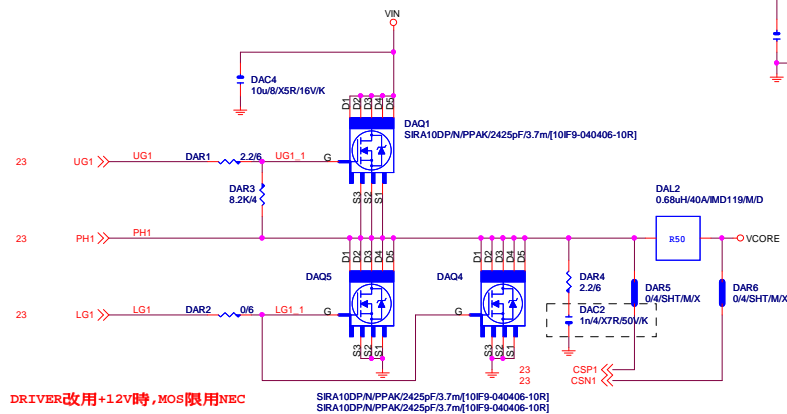
VCORE



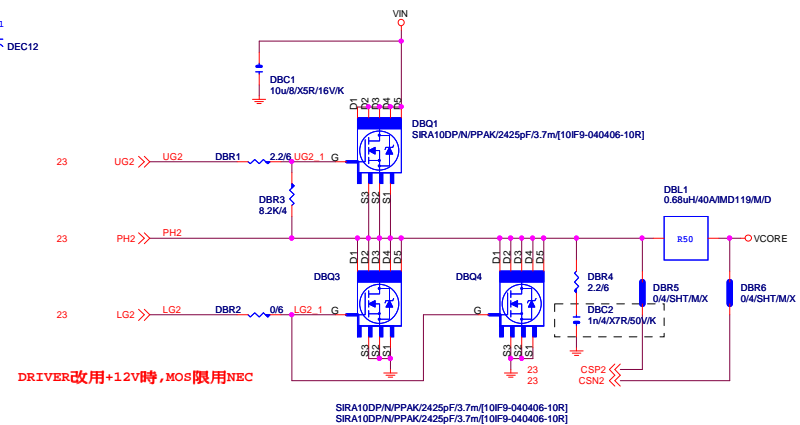
Gigabyte Technology			
Title VCORE_ ISL95820			
Size	Document Number		Rev
Custom	GA-P85-D3		1
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VCORE

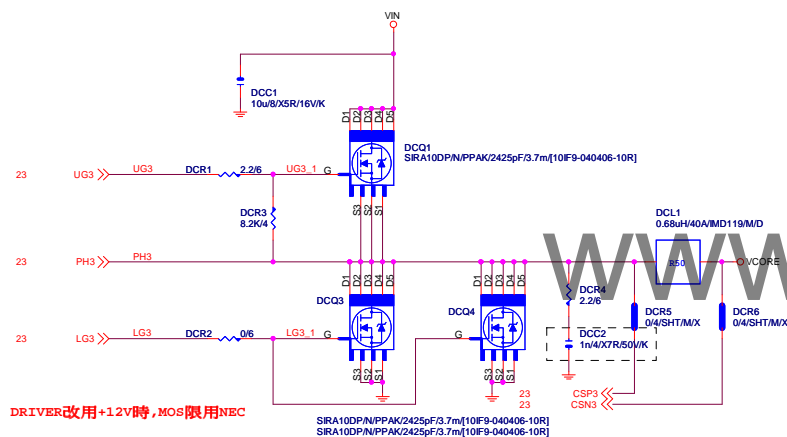
[1]



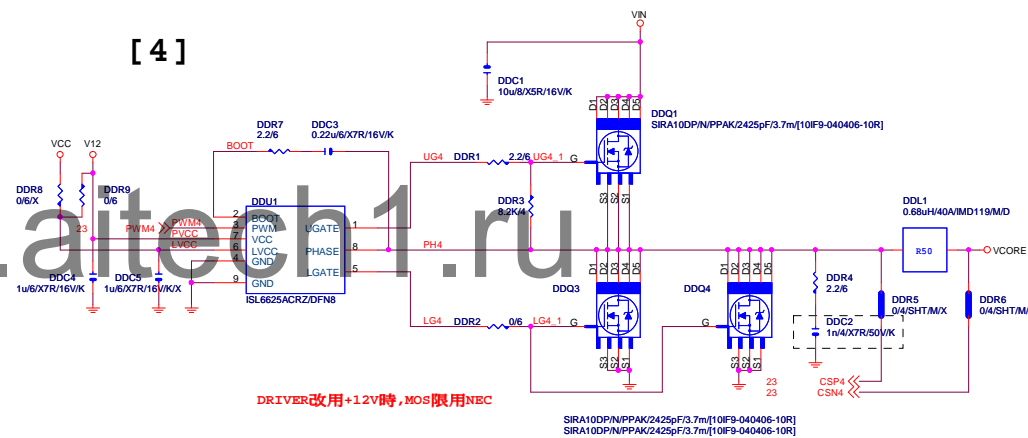
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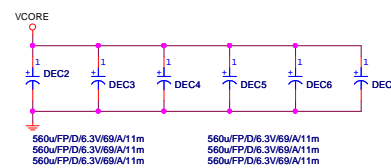
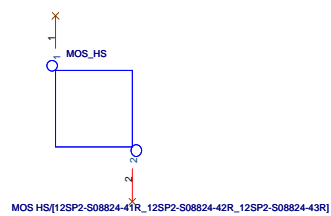
[3]



[4]

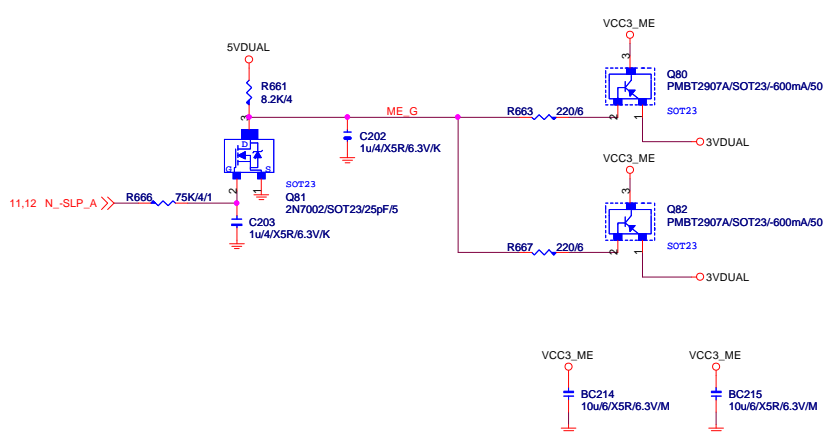


MOSFET HEATSINK

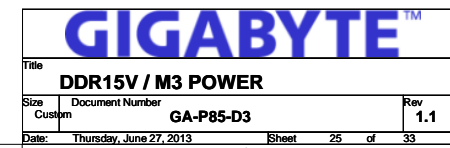
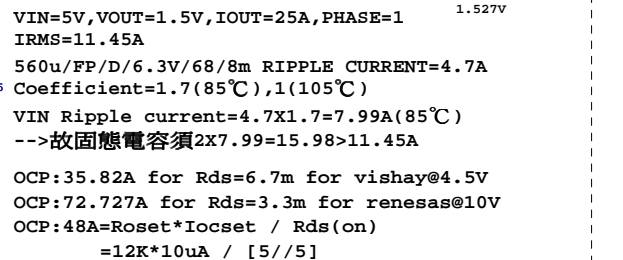


Gigabyte Technology			
Title	ISL95820_2		
Size	Document Number	GA-P85-D3	Rev 1.1
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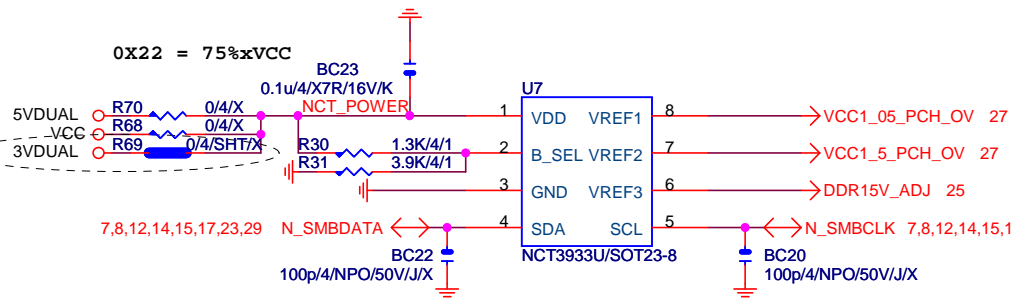
VCC3_ME



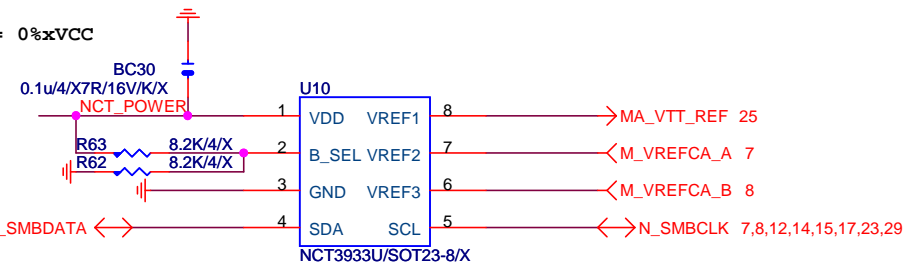
DDRVTT



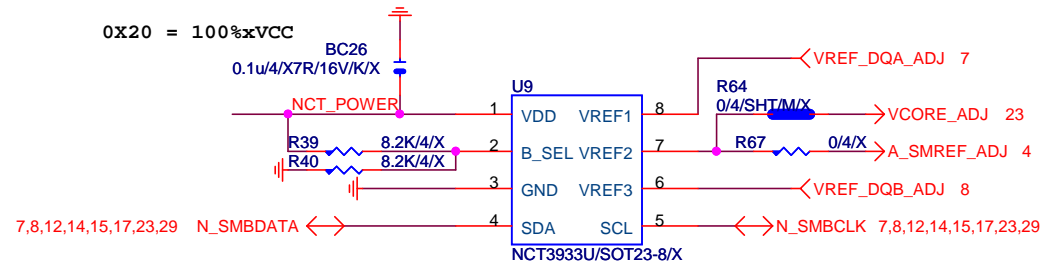
OVER VOLTAGE



0X2A = 0%xVCC



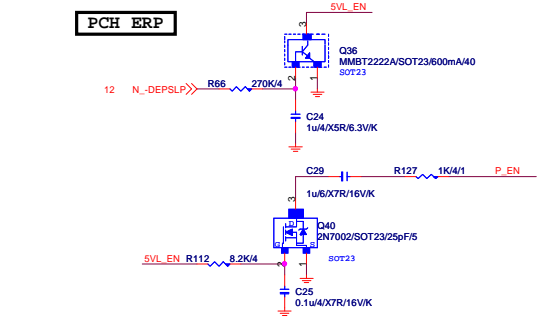
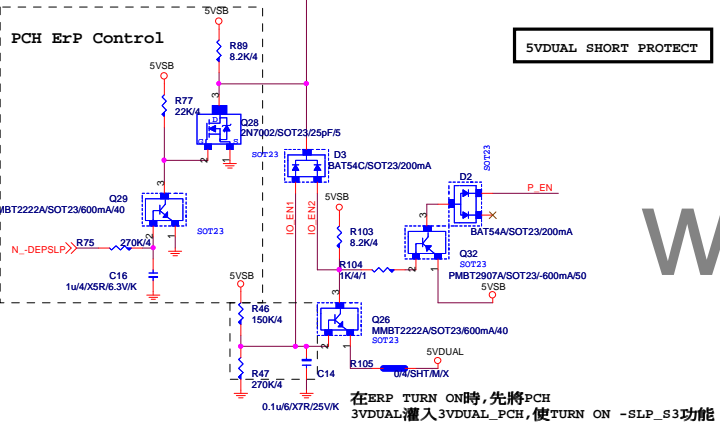
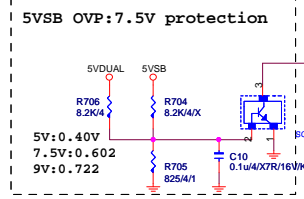
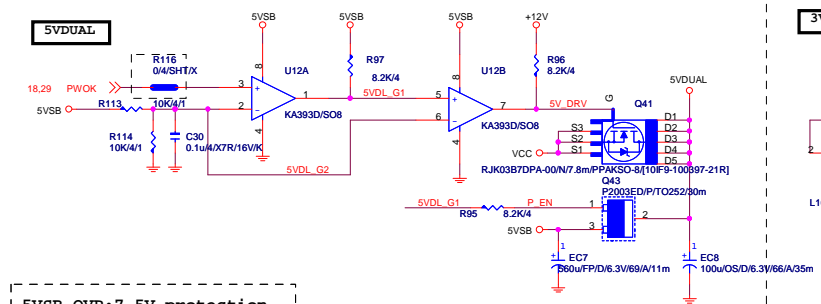
0X20 = 100%xVCC



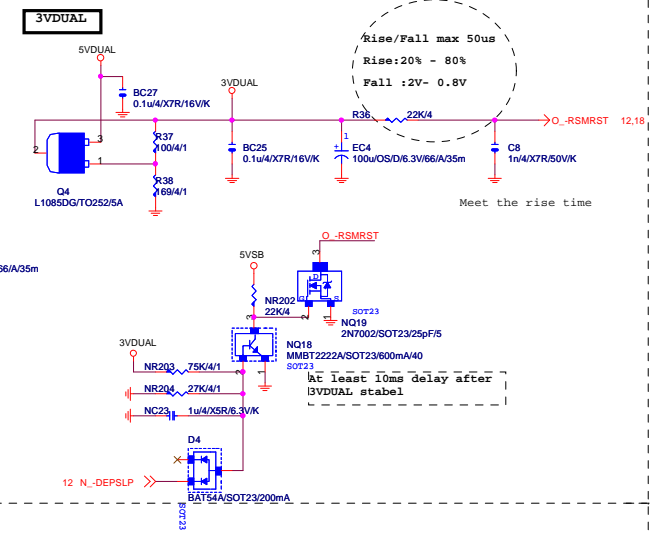
NCT3933	0X2A	0X20	0X22
VREF1	DDRVTT	VREF_DDRA_DQ	PCH Core
VREF2	VREF_DDRA_CA	N/A	VCC1_5_PCH
VREF3	VREF_DDRA_CA	VREF_DDRB_DQ	SMREF

Gigabyte Technology

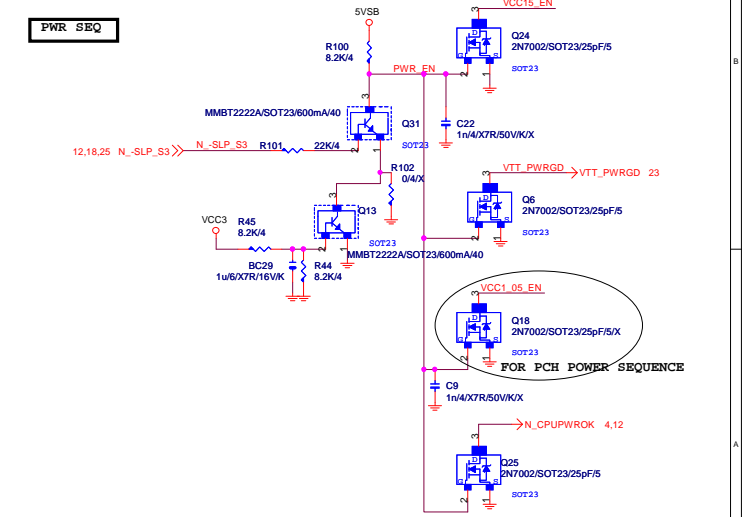
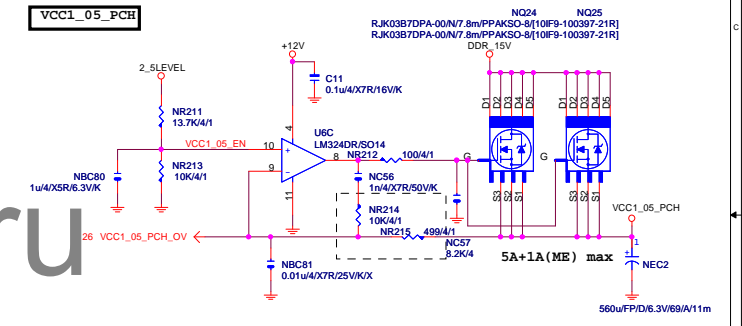
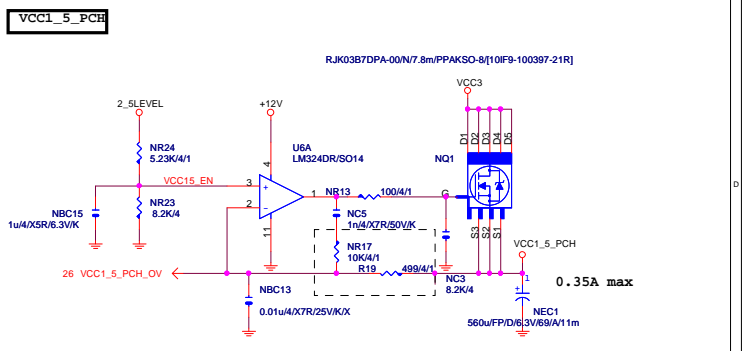
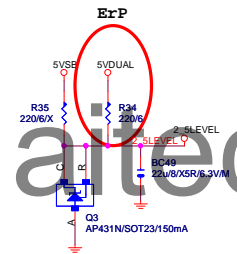
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CPU CORE VR-2		
Size	Document Number	Rev
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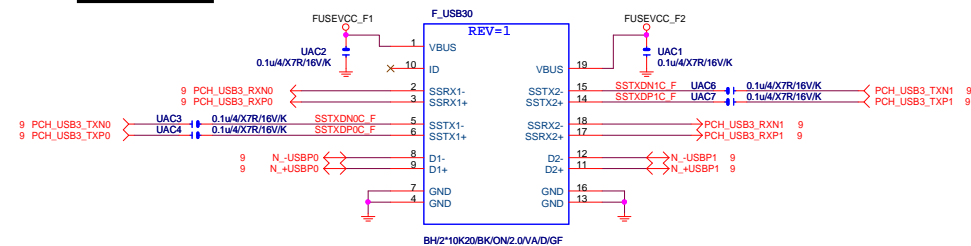
5VDUAL SHORT PROTECT



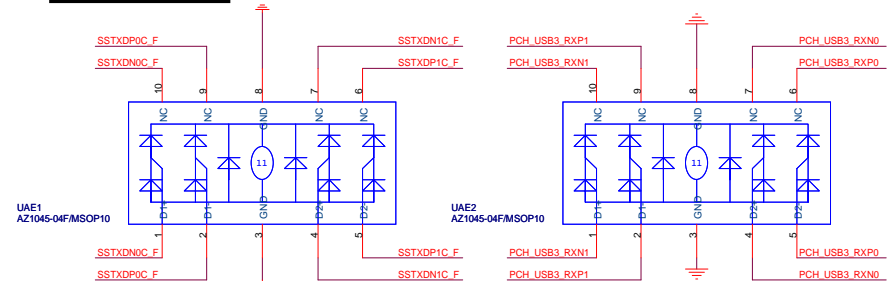
2_5LEVEL



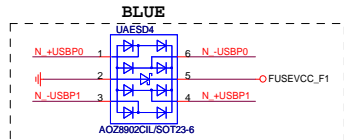
Front USB3.0



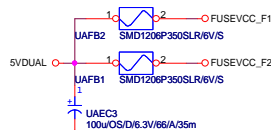
F_USB30 ESD PROTECT



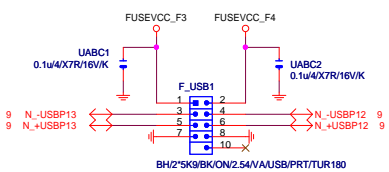
F_USB30 PWR



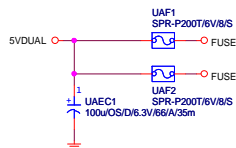
Close to connector



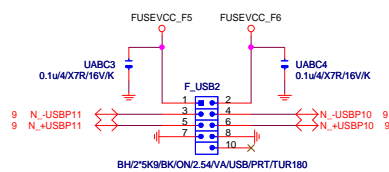
FRONT USB1



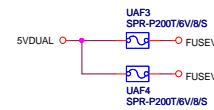
Close to connector



FRONT USB2

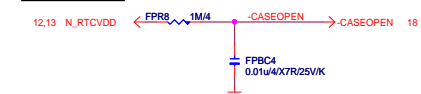


Close to connector

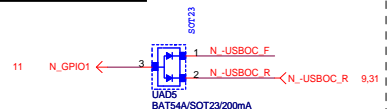


FRONT USB3

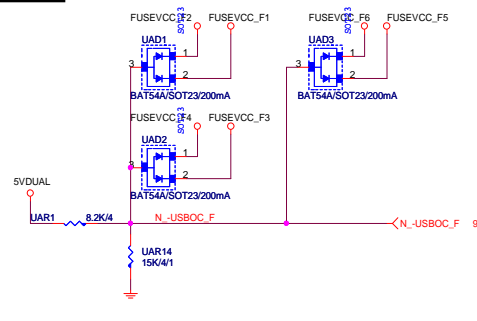
CASE OPEN



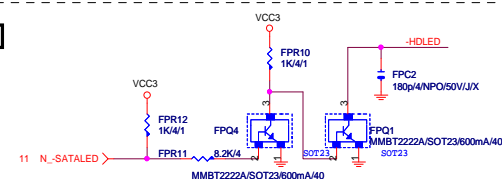
F_USB POWER PROTECT



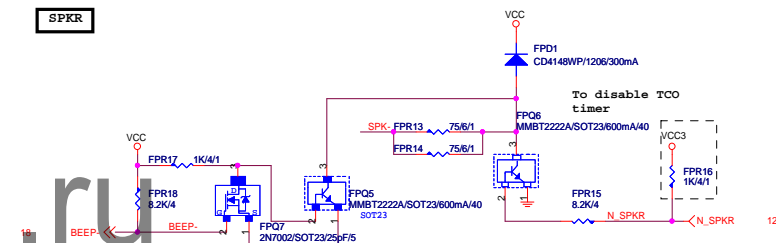
-USBOC_F



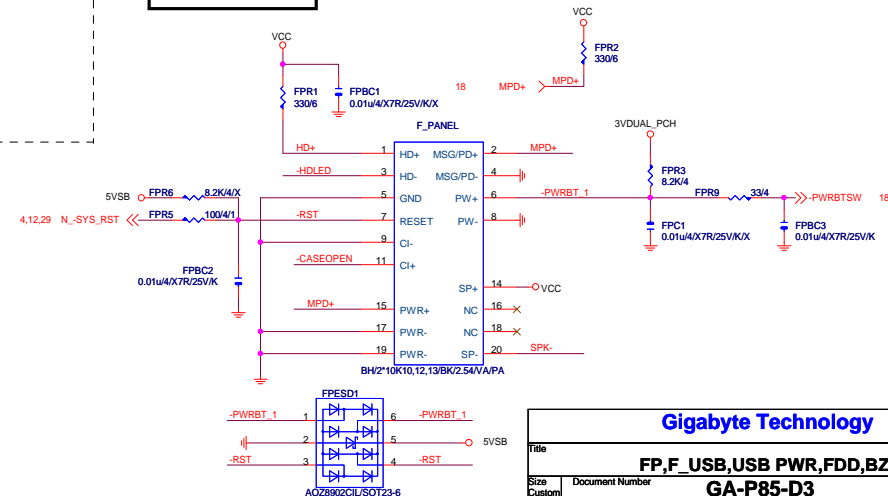
SATA LED



SPKR

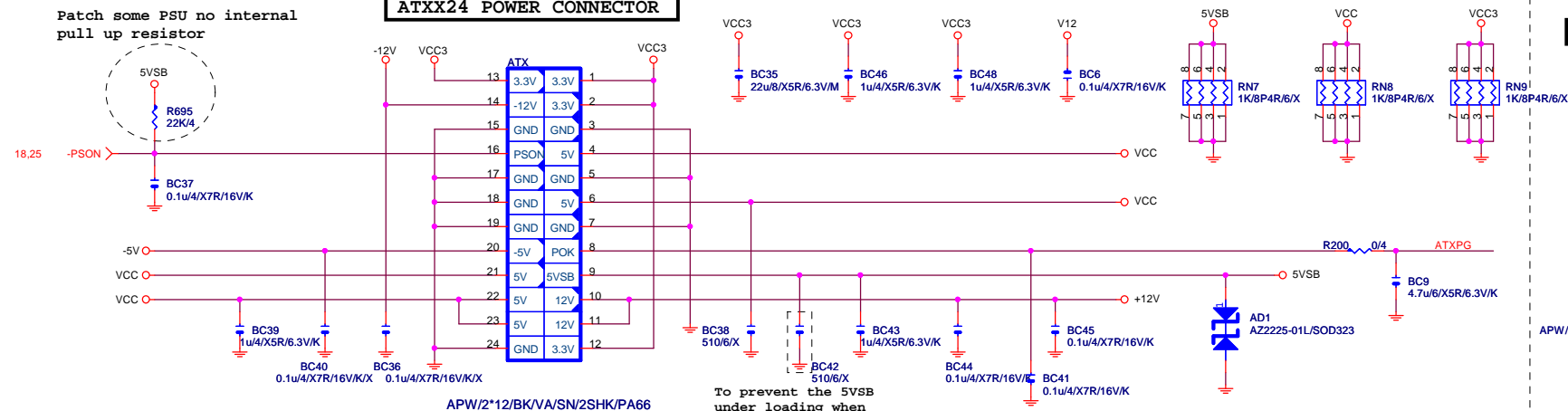


INTEL FRONT PANEL



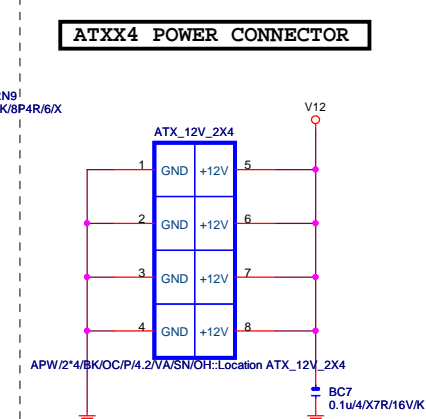
Patch some PSU no internal pull up resistor

ATXX24 POWER CONNECTOR

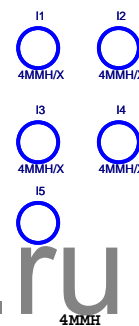
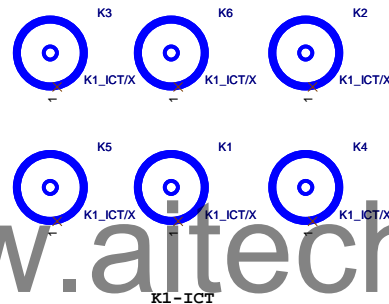
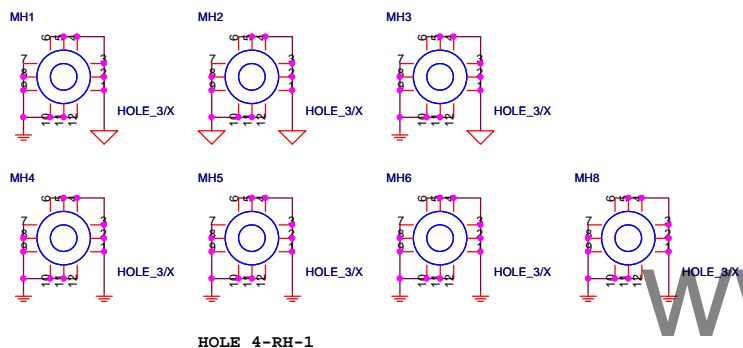


APW/2*12/BK/VA/SN/2SHK/PA66

ATXX4 POWER CONNECTOR

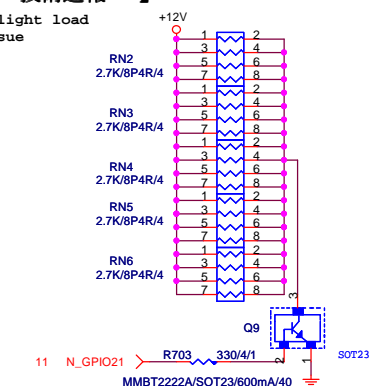


APW/2*4/BK/OC/PA/2/VA/SN/OH:Location ATX_12V_2X4



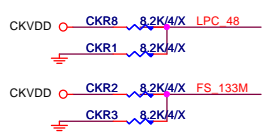
【技術通報R&D技術通報153】

To fix 12V light load abnormal issue

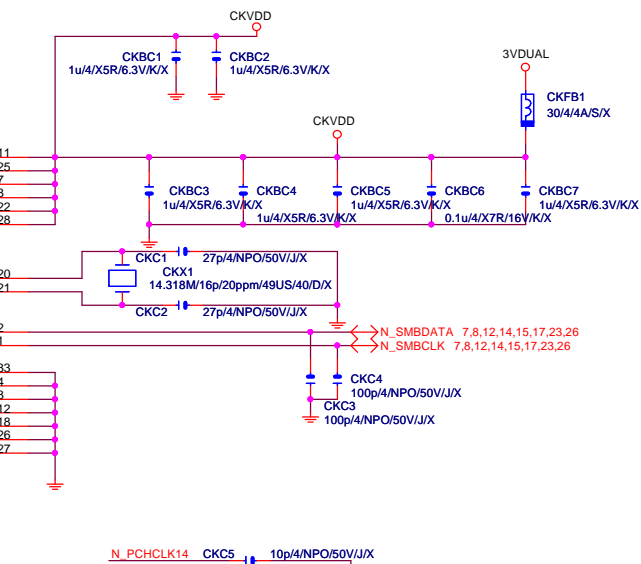
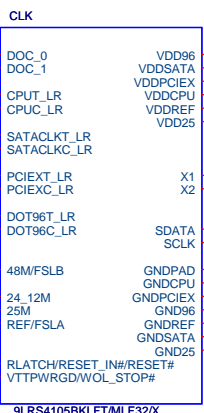
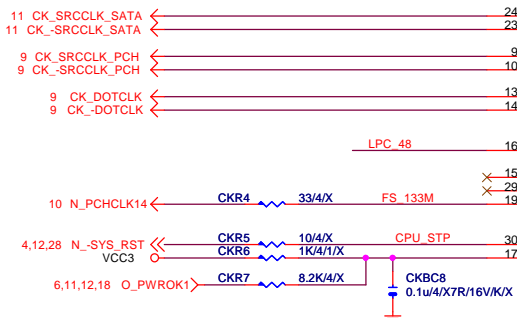


CLK GEN

CPU Frequency Selection

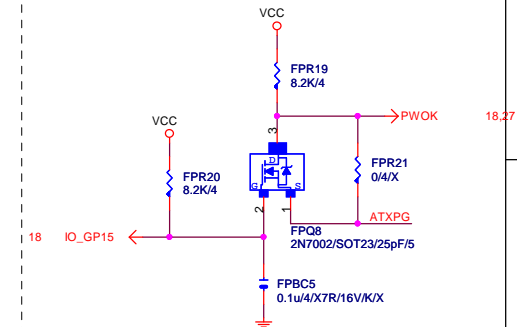


FSLB	FSLA	CPU
0	0	100M <Default>
0	1	133M
1	0	200M
1	1	166M



PWOK PATCH

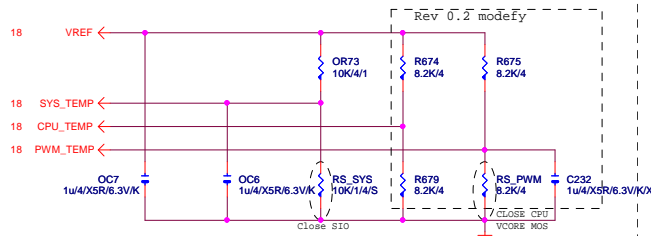
【技術通報R&D技術通報154】



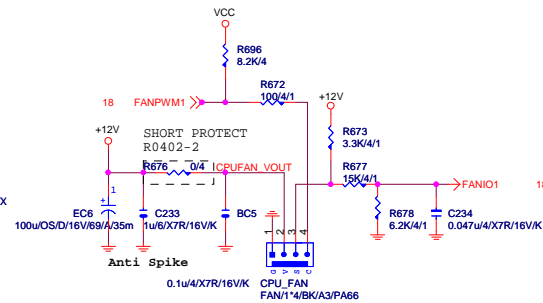
Gigabyte Technology

Title			ATX POWER CONNECTOR
Size	Document Number	GA-P85-D3	
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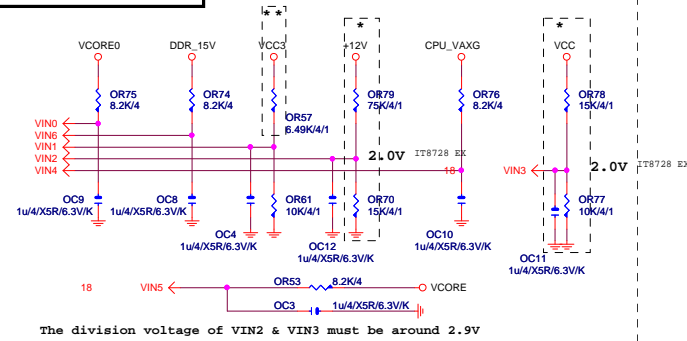
TEMP H/W MONITOR



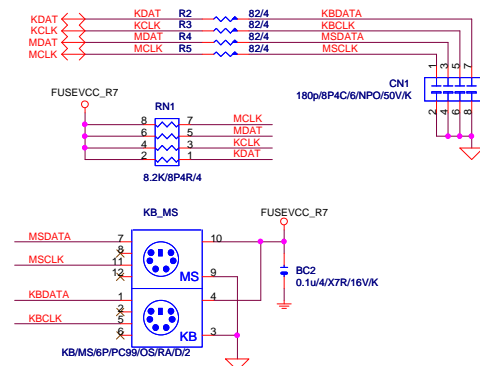
CPU SMART FAN



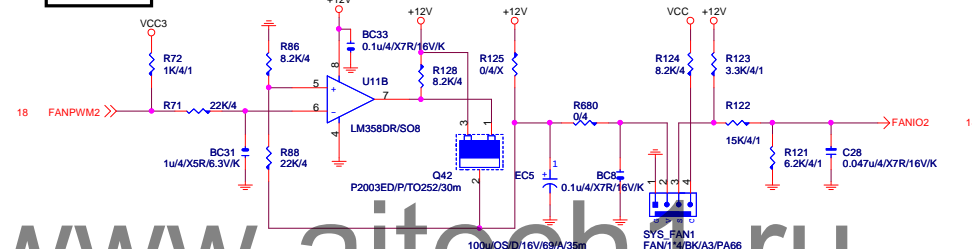
VOLTAGE-- H/W MONITOR



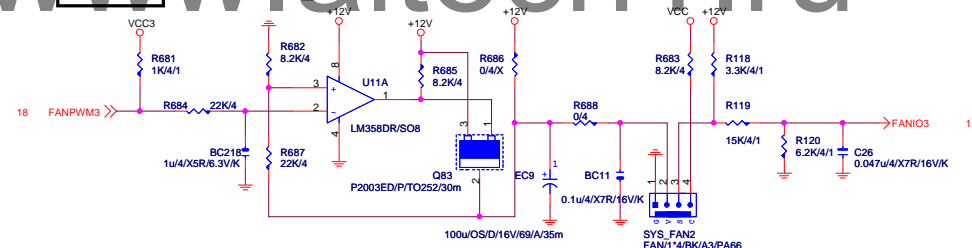
KB/USB



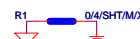
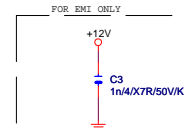
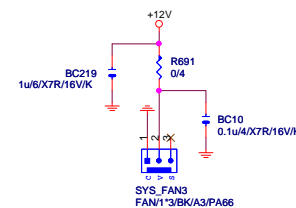
SYS_FAN_1 Linear SYS_FAN



SYS_FAN_2 Linear SYS_FAN



SYS_FAN_3 Linear SYS_FAN

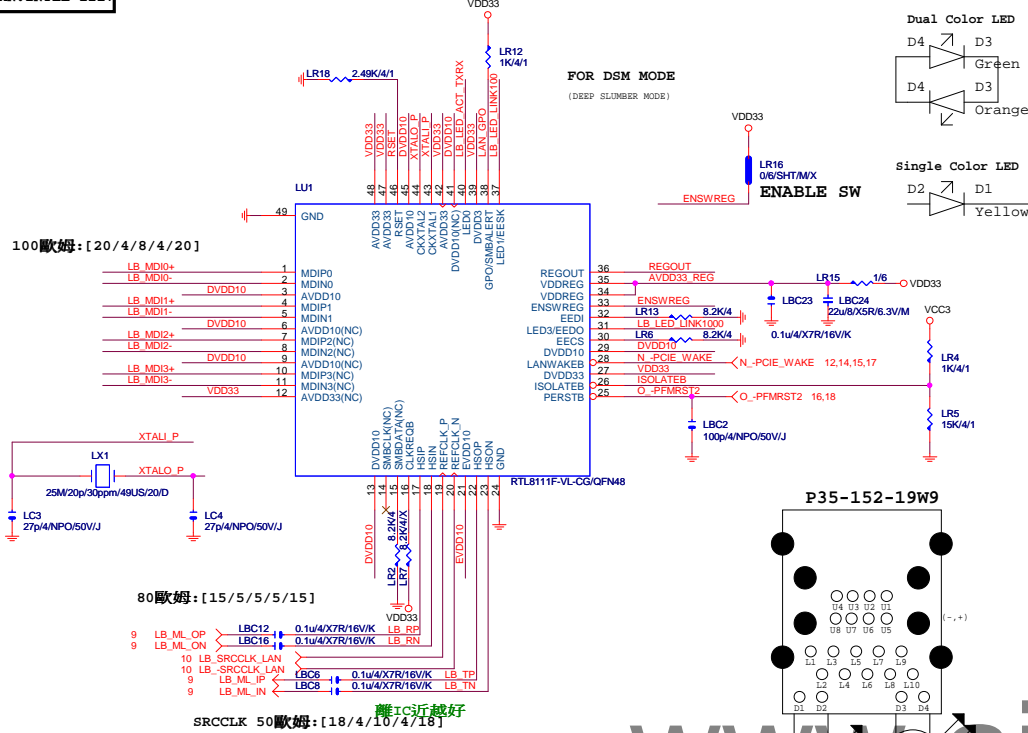


Gigabyte Technology

Title			HWM,KB/MS, FAN CTRL
Size	Document Number	Rev	
Custom	GA-P85-D3	1.1	
Date:	Thursday, June 27, 2013	Sheet	30 of 33

LAN:INTEL I217

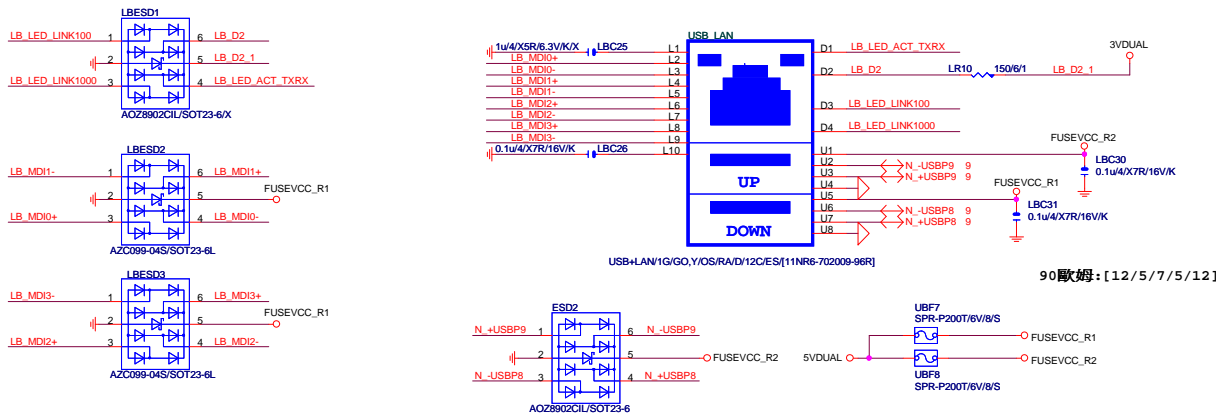
100歐姆:[20/4/8/4/20]



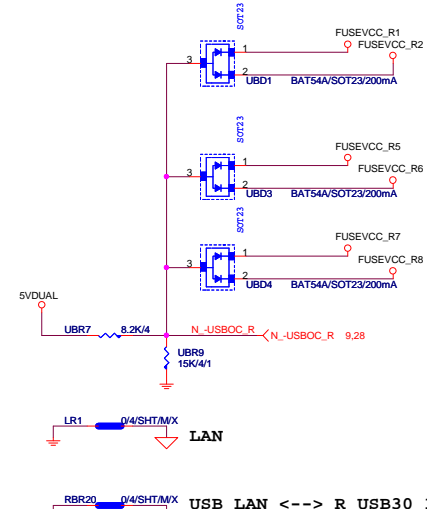
www.aitech1.ru

USB30_LAN CONNECTOR

100歐姆:[20/4/8/4/20]



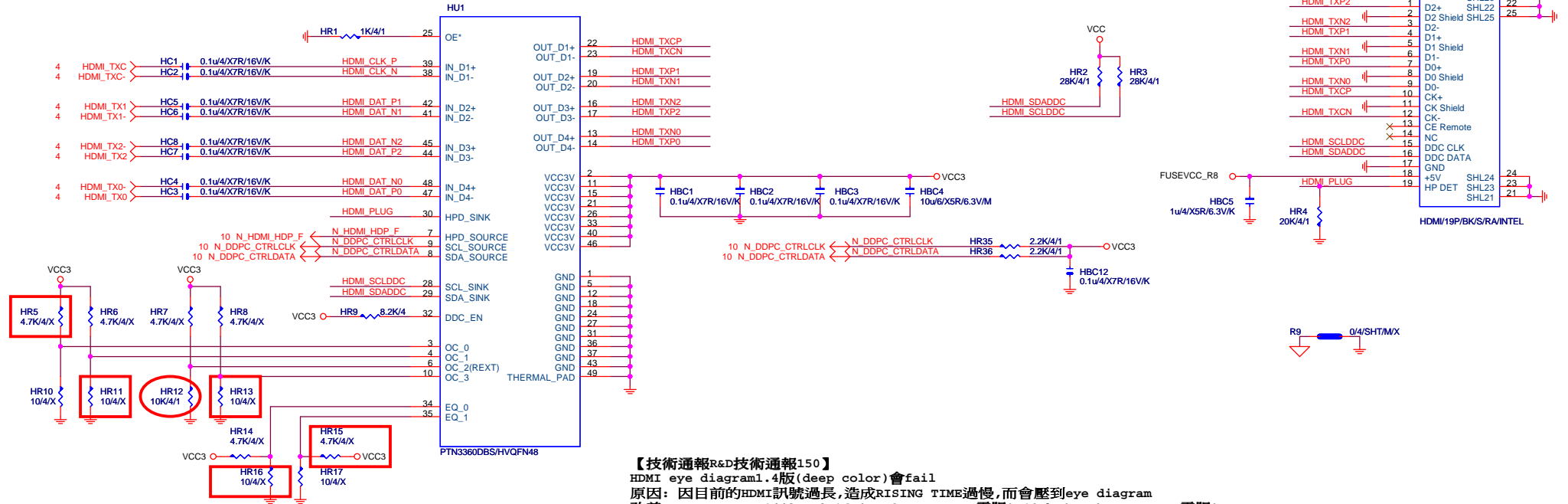
-USB0C_R



Gigabyte Technology			
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HDMI LEVEL SHIFT

HDMI:20/4/6/4/20
Impedance=85 +- 17.5%



PTN3360:PIN 4/10/34/35 NC PIN,都不上值;只上HR12:10K
ASM1442:紅色框要上,HR12:3.16K

GIGABYTE™			
Title HDMI			
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Super I/O ITE8720 GPIO Table

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PWM各相位的擺法如下：



Z77-D3H :
PCH :
12SP2-S05511-01R/02R/03R
MOSFET :
12SP2-S08924-01R/02R/03R

<i>Gigabyte Technology</i>			
Title			
TABLE LIST			
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